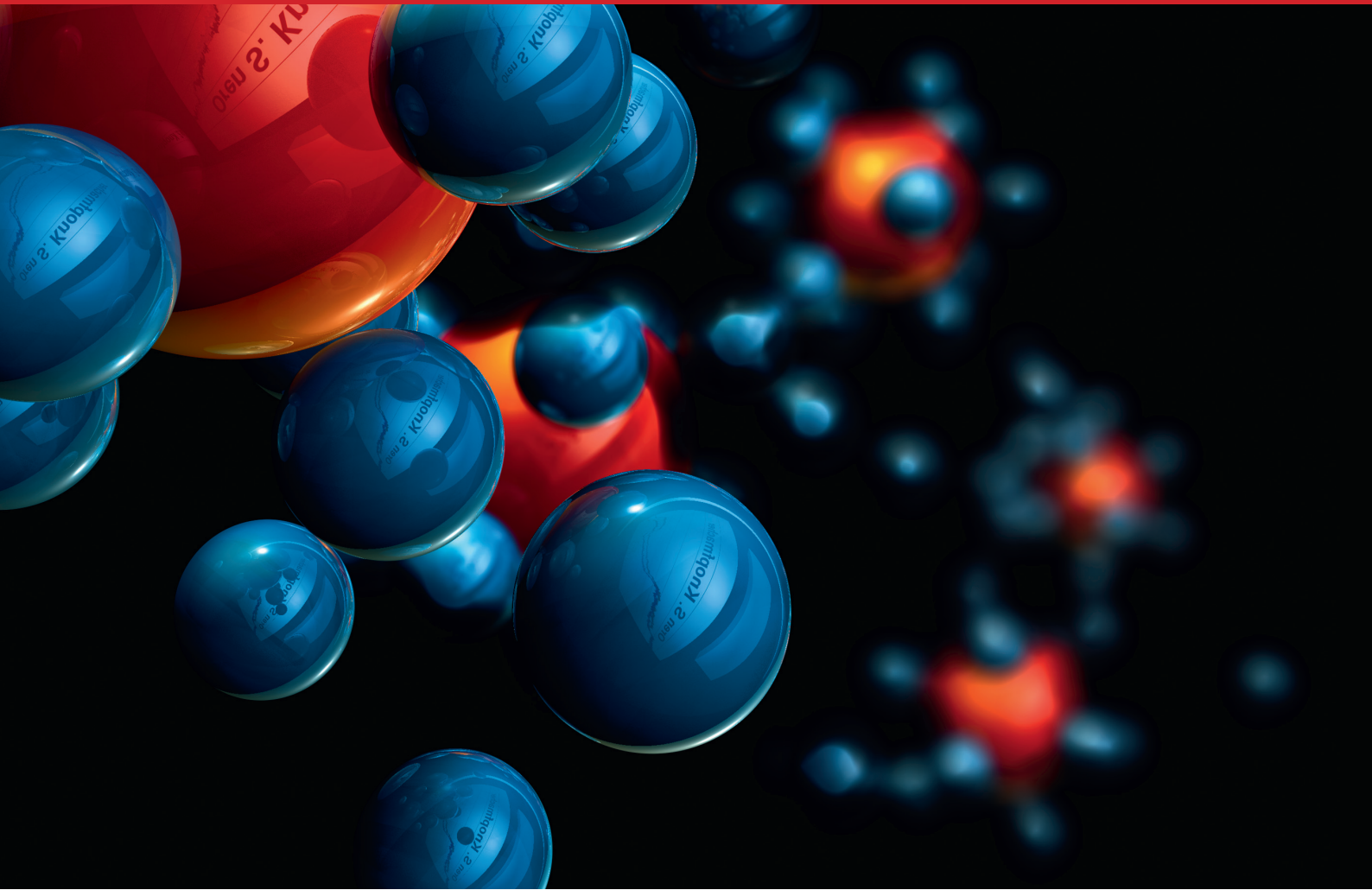
Oren S. Knopfmacher - **Sensing with Silicon Nanowire Field-Effect Transistors**



Sensing with Silicon Nanowire Field-Effect Transistors

Inauguraldissertation

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von

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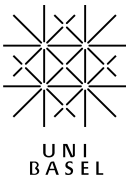

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auf Antrag von
Prof. Dr. C. Schönenberger
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Prof. Dr. A. Offenhäusser
PD Dr. M. Calame

Basel, den 21. Juni 2011

Prof. Dr. Martin Spiess
Dekan

One day Honi was going along the road, when he saw a man planting a carob tree. Honi asked, "In how many years will this tree that you are planting bear fruit ?" The man responded, "In seventy years." Honi asked, "Are you sure that you will live seventy more years to enjoy the fruit of this tree ?!" The man said, "I was born into a world with carob trees. Just as my ancestors planted for me, so I plant for my *descendants*."

Talmud Bavli Ta'anit 23,b

Cover layout designed by Matthias Triet – www.trickytriet.ch

Dedicated to those who believed in me, my family

"They're harmless when they're alone, but get a bunch of them together with a research grant and watch out."

Contents

Sensing – An Introduction

With the progress of modern biotechnology, current research efforts aim at medical diagnostic tools and personalized medicine to increase our overall quality of life [1]. Driven by this many innovations have already led to novel analysis tools currently used in the area of, e.g., drug discovery, proteomics or environmental monitoring. All these tools have a common working principle: convert a *biological* or *chemical* reaction into a *processable* and *quantifiable* signal [2]. For the time being two general strategies are employed to achieve appreciable sensitivity: *(i)* target-based amplification and *(ii)* signal-based amplification. In the first, a catalytic process can be used to increase the target analyte (e.g. the polymerase chain reaction[1]). Another option is labelling of the target and spectroscopic readout methods. However, such assay systems and techniques are costly, time-consuming and bear the risk of altering the target analyte. Another drawback consists in the lack in multiplexing capability. Multiplexing is known as the simultaneous detection of many agents, in other words selectivity. At present such medical diagnostic tools are highly centralized in laboratories which are equipped with complex instruments operated by highly skilled staff. Nowadays there is a growing need for portable, wearable and smart sensing devices for both point-of-care studies and for prolonged monitoring. Such sensors would offer rapid and portable analytical functionality in real-time, as well as low cost fabrication and massive multiplexing capabilities. However, the development of sensing systems that are reliable, label-free and cost-effective remains a challenging and unsolved task to date [3, 4].

During the past two decades the signal-based amplification has proven its ability to meet today's needs. It makes use of nano-scaled materials with their superior properties. Especially transducers built from such materials have a great potential as electronic (bio-)chemical sensors with molecular-level sensitivities due to their small size and their large surface-to-volume ratio, which is ultimately responsible for their high sensitivity [5]. Nanoscale electronic detection systems based on an ion-sensitive field-effect transistor implementation [6] are able to convert a *(bio-)chemical* signal into an *electrical* one, in plainer words, bringing together this two worlds in a smart

[1] Developed in 1983 and nowadays an essential technique in medical and biological labs.

way. Hence, CMOS-compatible nano-structured sensors will allow the high-density integration into a single diagnostic tool on chip – lab-on-chip – with a massive multiplexing degree of freedom. Nevertheless such a sensing platform requires a proper design meeting many demands, e.g., stability and differential readout capability with *in situ* references to prevent misreadings due to non-specific interactions and/or thermal drifts. Silicon nanowire field-effect transistors do have the potential to meet these boundary conditions. In contrast to carbon nanotubes which are semiconducting or metallic and are difficult to separate and graphene which has no (single layer) or a hardly tunable bandgap (multilayer), silicon nanowires can be seen as a promising choice. All signal-based assay systems have a common difficulty: controlling and understanding the interface between the transducer and the target agents is a crucial factor and needs to be carefully explored to allow reliable detection.

In this thesis we have worked towards a (bio-)chemical sensing platform realized by top-down fabricated silicon nanowire field-effect transistors. We will present measurements and results I have obtained during the past years in the nanoelectronics group of Prof. Christian Schönenberger at the University of Basel. Silicon nanowire field-effect transistors have been fabricated using state-of-the-art micro- and nano-fabrication methods.
To realize a reliable sensor, reproducible transistor characteristics have to be achieved in ambient environment. In **chapter 1** we introduce the silicon nanowire field-effect transistor, give an overview of the fabrication process and show necessary steps in order to achieve reproducibility. As a next step we describe in **chapter 2** investigations which were performed in order to achieve stable conditions in liquid environment. In **chapter 3** and **chapter 4** we focus on ion sensing experiments which were conducted along this thesis. Finally, in **chapter 5** we discuss additional investigations which are of importance for reliable detection of target analytes with our sensing platform. We will introduce the developed sensing platform realized with silicon nanowire arrays and conclude this thesis in **chapter 6**.

I hope the interested reader will enjoy our excursion into the world of electrical sensing with silicon nanowire field-effect transistors.

1

Si Nanowire FETs: From Fabrication to Function in Ambient Environment

1.1 The Transistor - An Introduction

A transistor is a device made from a semiconductor material and is applied to amplify or switch an electronic signal, comparable with a valve for controlling a supply of water. Shortly after its invention in 1947 (Fig. 1.1a) it became a basic building block for integrated circuits with many applications [7]. In general, there are two main types of transistors – bipolar (junction) transistors and field effect transistors (FET). In this thesis we study a special kind of field effect transistor realized by a top-down fabricated silicon nanowire. In the following section we will provide a basic introduction into its theory. Details can be found in appendix B and C and the standard literature, e.g. Sze [8], Van Zeghbroeck [9] or Colinge [10]. Please note that parts of the theory have been slightly adapted from the standard literature.

1.1.1 The MOSFET

The most commonly used transistor in today's integrated circuits is the metal oxide semiconductor field effect transistor (MOSFET). It was firstly proposed in 1959 by Moll, Pfann and Garrett [8] and has been extensively studied in the literature. A typical n-type MOSFET is sketched in Fig. 1.1b.

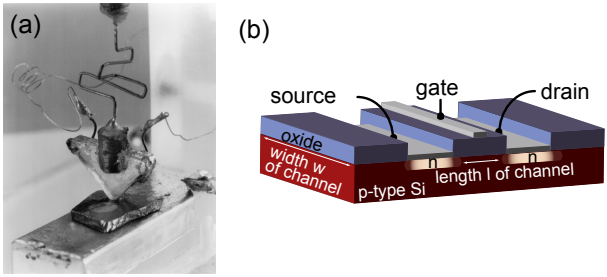


Figure 1.1: **(a)** First transistor fabricated 1947 at Bell Labs. **(b)** Schematics of a n-type MOSFET device.

It consists of two highly conducting n-doped source and drain regions, isolated from the p-type substrate below them. A metal gate on the surface is separated from the semiconductor by an insulating oxide layer. The terminals of a FET are labelled gate, source and drain. While applying a voltage to the source and drain contacts, a current is able to flow between them, forming a conductive channel with width w and length l (Fig. 1.1b). If a voltage is applied to the gate, the current in this channel is modulated by the resulting electrical field (Fig. 1.2a), hence, by altering the gate voltage the conductive channel is electro-statically changed and hence its conductivity. By means of this effect a FET can control the flow of electrons (n-type semiconductor) or holes (p-type semiconductor). For small bias voltages, V_{sd}, between source and drain (inset of Fig. 1.2a) the current I_{sd} increases linearly with applied V_{sd}, also known as the linear regime. To tune the current in the conductive channel, a gate voltage V_g can be used. If a certain gate voltage must be applied in order to allow a current to flow (Fig. 1.2b), the MOSFET is known as enhancement-mode or normally-off.

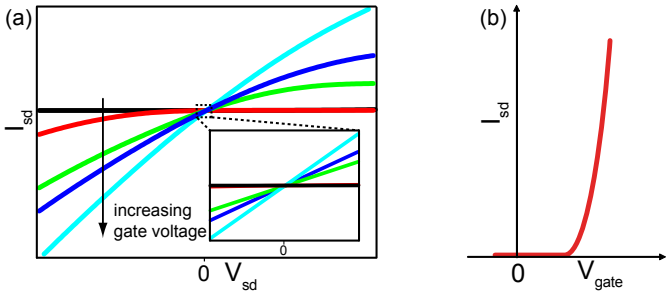


Figure 1.2: **(a)**Revised measurement of a graph displaying the source-drain bias current I_{sd} vs. applied source-drain bias voltage V_{sd}. The inset shows the linear region. **(b)** Simplified graph showing I_{sd} vs. applied gate voltage V_{gate} characteristics of a MOSFET.

For small V_{sd} the MOSFET behaves as variable linear resistor. We can describe the flowing source drain current I_{sd} as the total charge Q per unit area induced in the channel $w \cdot l$ which needs the time τ to flow from source to drain

$$I_{sd} = \frac{Qwl}{\tau}. \tag{1.1}$$

Here the gate has a width w and a length l (Fig. 1.1b). If we assume the charge carrier flow velocity which equals the product of the carrier mobility μ and the applied electric field E $(= V_{sd}/l)$ to be constant over the channel length, we can rewrite this velocity as

$$\nu = \mu \frac{V_{sd}}{l}. \tag{1.2}$$

The induced charge carriers Q per unit area can be described as the product of the gate capacitance per unit area, $C_g^{'}$, and the applied gate voltage, V_g. With equations (1.1) and (1.2), a constant charge carrier density and a constant electric field as a direct consequence of the constant velocity of the charge carriers we arrive with the source drain current to be:

$$I_{sd} = \mu \frac{w}{l} Q V_{sd} = \mu \frac{w}{l} C_g^{'} V_g V_{sd} \tag{1.3}$$

This is the most basic transistor relation and holds for the linear regime of the transistor. Next we will focus on the semiconductor-oxide interface to understand the device operation of the MOSFET (for details see appendix C, page 105).

1.2 MOS capacitance analysis

If a semiconductor is brought into contact with a metal, being only separated by an insulator (Fig. 1.3a), the band of the semiconductor will bend (Fig. 1.3b). To correct for this effect and to obtain 'flat-band' condition (Fig. 1.3c), a finite gate voltage V_{fb} needs to be applied (for details see appendix C on page 105).

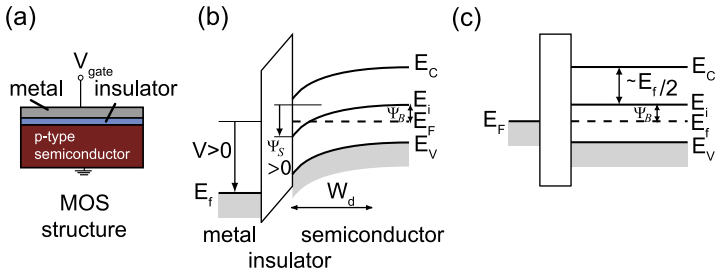


Figure 1.3: **(a)**Metal oxide semiconductor structure (MOS). **(b)** Band structures in weak inversion. **(c)** Band structures of a MOS for a p-type semiconductor structure with flat-band condition. Notations are given in appendix C on page 105. Adapted from [11].

Basically three main physical states exist at the semiconductor-insulator. When a negative voltage is applied the bands' bending cause an accumulation of majority carriers (in our case holes for a p-type semiconductor) near the semiconductor-oxide interface. This case is called accumulation (Fig. 1.4a).

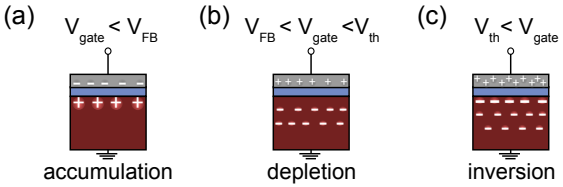


Figure 1.4: **(a)** Charges of the sketched MOS under accumulation, depletion **(b)** and inversion **(c)** conditions.

If a small positive voltage is applied we start to deplete the majority carriers, hence it's known as depletion case (Fig. 1.4b). The majority carriers

are pushed into the substrate and there are no mobile charges left. If we even further increase the voltage to more positive values, we start to accumulate minority carriers (electrons) at the interface. At sufficiently large voltages the number of the minority carriers at the surface is larger than the majority carriers and the surface is hence inverted. This case is therefore called inversion (Fig. 1.4c). If the applied voltage crosses a certain threshold value, V_{th}, a current will start to flow again. This is the inverted situation. V_{th} is one of the most important parameter of the MOS transistor. It is defined as the voltage that must be applied in order to turn the transistor on [8] (for details see appendix C, page 108). Below the threshold voltage the charge in the channel is zero. The threshold voltage can be either positive or negative, depending on the doping concentration of the substrate and the gate electrode. With this knowledge equation (1.3) can be rewritten as

$$I_{sd} = \mu \frac{w}{l} Q V_{sd} = \mu \frac{w}{l} C_g^{'} (V_g - V_{th}) V_{sd}. \tag{1.4}$$

1.3 Subthreshold regime

When the gate voltage is below the threshold voltage (and the surface of the semiconductor is in 'weak' inversion) the drain current below threshold is called subthreshold current and we are in the subthreshold regime (Fig. 1.5). This current is independent of the source-drain bias and suggest that its a diffusion driven process. The free-electron density in the channel is described by Boltzmann statistics $n = n_i e^{-e\psi_S / k_B T}$ with n_i the intrinsic carrier concentration, k_B the Boltzmann constant, T the temperature, e the elementary charge and ψ_S the surface potential at the semiconductor-insulator interface. The carrier density of this small subthreshold current, integrated over the depletion width W_d, $Q = \int_0^{W_d} n(x)dx$ can be calculated to be [8, 12]

$$Q = \frac{k_B T}{e} \sqrt{\frac{\epsilon_s \epsilon_0}{2 e \psi_S N_A}} n_i e^{\frac{e\psi_S}{k_B T}} \tag{1.5}$$

ϵ_s and ϵ_0 denote the permittivity of the semiconductor and the vacuum and N_A the acceptor concentration. This equation indicates the exponential dependency of the subthreshold current on ψ_S [8]. We introduce here a parameter which expresses how sharply the transistor is turned off by the gate voltage. The subthreshold swing, S, is defined as the gate voltage that is needed to increase the subthreshold current by one order of magnitude

$$S = \frac{dV_g}{d\log(I)} = \ln(10) \frac{dV_g}{d\ln(I)} = 59.5\,\mathrm{mV} \left(\frac{C_D + C_{ox}}{C_{ox}} \right) \tag{1.6}$$

The term $(C_D + C_{ox})/C_{ox}$ is related to the applied gate voltage drop; over the insulator and partially within the semiconductor (appendix C, page 108). C_D denotes the depletion layer capacitance and $C_{ox}$the insulator capacitance, both per unit area. The lower the value of S, the more efficient and rapid the switching of the device from the off state to the on state reaching its minimum at $\sim 60\,\mathrm{mV/dec}$ (300 K).

1.3.1 Transfer characteristics

The transfer characteristics of an FET can be obtained by applying a constant source-drain voltage and varying the gate voltage. The monitored source-drain current plotted against the applied gate voltage reveals its behaviour. Fig. 1.5a shows a sketched example of a transfer characteristic of a p-channel FET. Previously introduced parameters like threshold voltage V_{th} and subthreshold swing S can be extracted. Here, V_{th} is determined in the linear region by the gate-axis intercept of a tangent to the $\mathrm{I}(V_g)$, taken at the inflection point. The slope of the fit defines the transconductance $g_m = dI_{sd}/dV_g$. An FET device that operates either as p- (holes) or n- (electrons) channel device is known as unipolar transistor. In the case where both, electrons and holes, can be injected as charge carriers into the channel, one observes an ambipolar behaviour.
Fig. 1.5b sketches the transfer characteristics for an ambipolar transistor with holes as majority carriers. As discussed previously the three regimes, accumulation, depletion and inversion are visible. For negative gate voltages, holes are accumulated in the channel (Fig. 1.4b). At a certain less negative gate voltage the amount of holes decreases until the accumulated charges in the channel equals zero. Below $\mathrm{V}_{th,p}$ the channel is depleted (Fig. 1.4c) and a depletion layer is formed. The current in the channel is exponentially suppressed. When the gate voltage crosses a certain positive gate voltage $\mathrm{V}_{th,n}$ (Fig. 1.4d) the channel is inverted and the current starts to flow again.

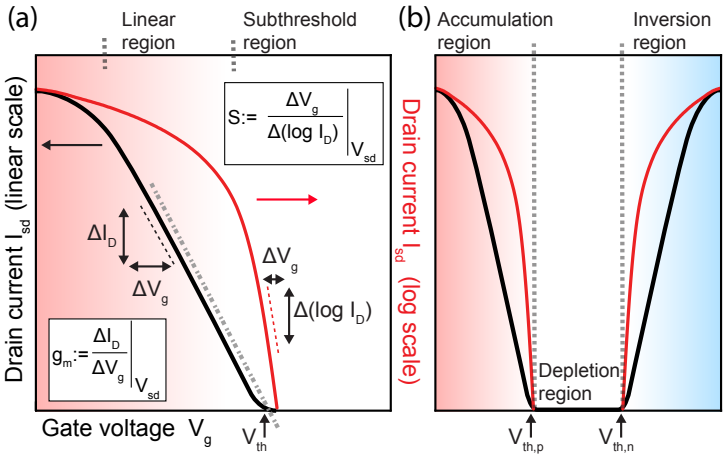


Figure 1.5: **(a)** Sketch of typical transfer characteristic of a p-channel FET showing the source-drain current as a function of applied gate voltage in linear (black, left axis) and logarithmic (red, right axis) representation. The vertical dashed lines indicate the different regions. The threshold voltage V_{th} is determined by the gate-axis intercept of a linear fit to the $I_{sd}(V_g)$, taken at the inflection point. The change of the source-drain voltage for a given change in the gate voltage in the linear region is known as transconductance g_m. The subthreshold swing S is extracted by a linear fit of the source-drain voltage in log scale at the subthreshold region. **(b)** Ambipolar behaviour of a p-channel FET. The graph can be divided in three regions: accumulation, depletion and inversion. The threshold voltages for the accumulation $V_{th,p}$ and inversion $V_{th,n}$ region are indicated (vertical arrows).

1.3.2 From conventional MOSFETs to Silicon Nanowire FETs

With the need for faster and smaller electronics, semiconductor industry faces problems with the realization of conventional MOSFETs. Since scaling theory predicts decreasing dimensions of the FETs [13, 14, 15, 16], (1D) nanoscale structures may have the possibility to break this barrier. Nanostructured FETs made from carbon nanotubes [17, 18], graphene [16] or silicon nanowires [19, 20] exhibit excellent electronic properties and may be seen as ideal building blocks for nanoelectronic applications. In contrast to carbon nanotubes with metallic or semiconducting properties and graphene (no bandgap for a single layer), silicon nanowires have the advantage of being only semiconducting and may be more easily integrated into CMOS industry fabrication and processing. The main difference to the conventional

MOSFET channel (Fig. 1.6a) is the fact, that the nanowire itself serves as conductive channel, connected by source and drain contacts (Fig. 1.6b). A substrate underneath the nanowire can be used as back gate, electrically isolated by an insulator.

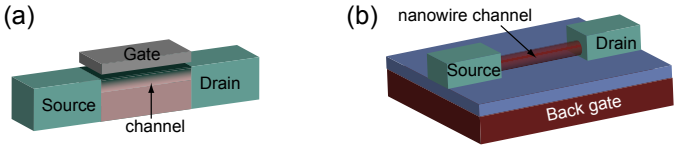


Figure 1.6: **(a)** Sketch of the conductive channel of a MOSFET. **(b)** In contrast to a conventional MOSFET, the whole nanowire can be seen as conductive channel.

1.4 SiNW FETs: From fabrication to functional devices

All devices investigated in this thesis were fabricated following the top-down approach first introduced by Reed et al. [21]. By making use of this process the whole structure can be designed and transferred into a silicon-on-insulator wafer (SOI), using state-of-the-art micro- and nanofabrication techniques. The top-down techniques allow the production of many devices with the same or similar properties, while giving the possibility for precise patterning and high resolution.

1.4.1 Fabrication flow

Fig. 1.7 summarizes the fabrication steps. Details of the fabrication process can be found in appendix B. All devices were fabricated by selectively dry and wet etching different layers of a <100> SOI wafer [22, 23]. A SOI wafer consists of three layers: the device layer, a sandwiched middle buried oxide (BOX) layer, and the bottom layer, also named substrate or handle wafer (Fig. 1.7a). If not otherwise mentioned low boron p-doped SIMOX SOI wafers with a resistivity of 10–20 Ωcm were used, which corresponds to a doping density of $\sim 10^{15}\,\mathrm{cm}^{-3}$. The unprocessed SOI wafer consists from top to bottom of a 100 nm thick silicon device layer (t_{device}), a 150 nm thick BOX layer (t_{box}) and the 500 μm thick silicon substrate (Fig. 1.7a). Several SOI wafers were used in this thesis. The device layer was thinned to a thickness between 60–80 nm by thermal oxidation leaving a top SiO_2 layer of 40–80 nm (t_{tox}).

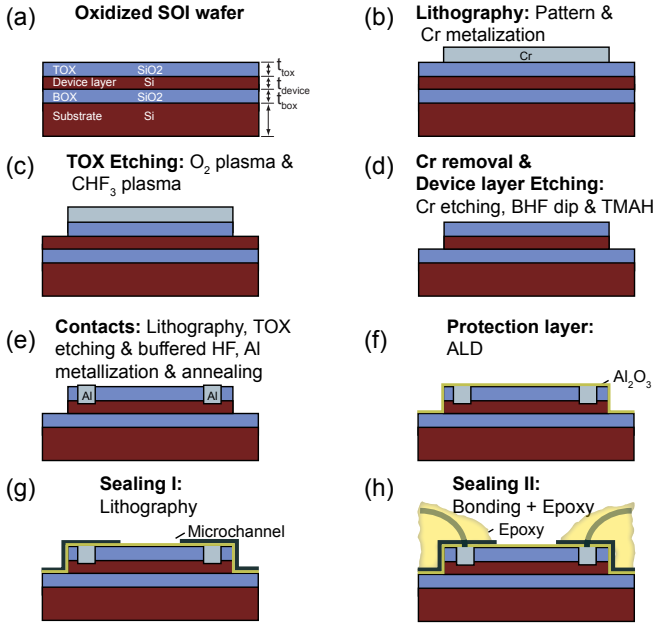


Figure 1.7: Summary of the fabrication process (details of the fabrication process can be found in appendix B): **(a)** As starting material we use an SOI wafer with a thermally grown top SiO_2 layer. **(b)** The structure is defined either by e-beam or UV lithography and chromium evaporation. **(c)** The pattern is then transferred into the TOX layer by CHF_3 and O_2 plasma etch. **(d)** After removing the chromium layer the device layer is etched in a TMAH etching solution. Hereby the patterned TOX layer acts as an etching mask. **(e)** To contact the fabricated SiNWs contact structures are patterned by UV lithography. Then the TOX layer is removed at those areas using buffered HF. Aluminum is deposited and annealed to form ohmic contacts. **(f, g)** For measurements in liquids (cf. chapter 2) an Al_2O_3 atomic layer protection layer is deposited. Then a micro-sized liquid channel is defined by UV lithography. **(h)** As final steps the device is glued into a chip carrier, bonded and sealed with an insulating epoxy. Details of the fabrication process are described in appendix B.

The top oxide (TOX) layer acts as etching mask and protecting layer for the leads working in liquid environment[1].

[1] Thermal oxidation was performed by the LMN group at the Paul Scherer Institute.

1.4.2 Fabrication of SiNW FET devices

Fig. 1.8 shows the main two structures which were designed, produced and measured. In a single manufacturing process a batch was fabricated containing several devices (Fig. 1.8a). A device is built up of several nanowires including contact leads, bonding pads and, if needed, on-chip electrodes for local gating of the nanowire FETs (Figs. 1.8b and 1.8c).
To fabricate nanowire devices both, e-beam and UV lithography techniques were used. The shape of e-beam written nanowires could be varied with dimensions between 0.1 μm-1 μm in width and 1 μm-1 mm in length. Several hours were necessary in order to pattern one batch containing 4 to 6 devices due to the slow e-beam process. To decrease overall fabrication time we replaced the e-beam lithography by an UV lithography process which allows to increase the device-output. Dimensions of UV lithography fabricated wires were limited by the resolution of the mask aligner (MJB-4) and the patterns on the glass masks. Nanowire structures on the fabricated mask had dimensions of 0.5–1.5 μm in width and 10 μm in length. The device sketched in Fig. 1.8b was produced via a combination of e-beam and UV lithography. While e-beam lithography was used to write wires and contact leads, UV lithography was used to pattern contact pads. The structure contained seven nanowires which could vary in width and length. In Fig. 1.8c the number of nanowires was decreased in order to add on-chip electrodes. Here patterns were produced by means of UV lithography only.

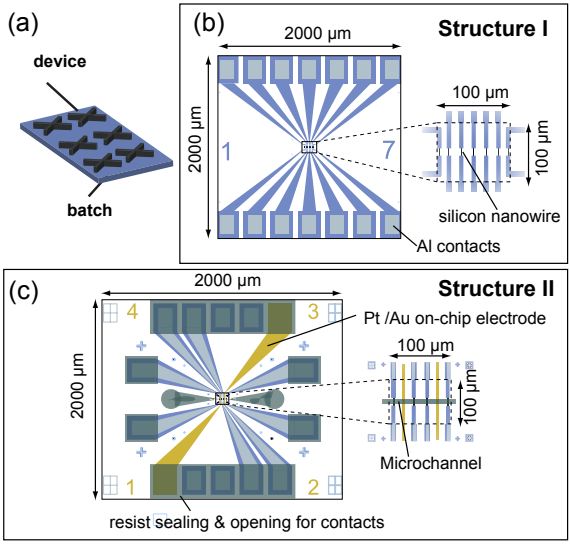


Figure 1.8: Schematics of the lithography masks: **(a)** Throughout a fabrication process one batch was fabricated which contains several devices. **(b)** Structure I was patterned by e-beam and UV lithography. Parts of contact leads (violet) and contact pads (gray) were patterned via UV lithography while the nanowires (black) and the inner connection leads were patterned by e-beam lithography. The width of wires could be varied. **(c)** Structure II was patterned by UV lithography only. Platinum, respectively gold on-chip electrodes could be integrated as local gates. To prevent leakage currents a micro-channel was structured via UV lithography.

Figs. 1.9a, 1.9b and 1.9c show optical images of different fabricated structures. The final width of the nanowires varied between ∼100-1000 nm depending on used lithography process and wet etching times. For e-beam written nanowires [11] typical widths are ∼100 nm (Fig. 1.9d), while for wires produced via UV lithography we found widths of typically ∼ 700 nm-1 μm (Fig. 1.9e). By reasons of the anisotropical wet etching process silicon nanowires form a trapezoidal shape (Fig. 1.9f, appendix B, page 91).

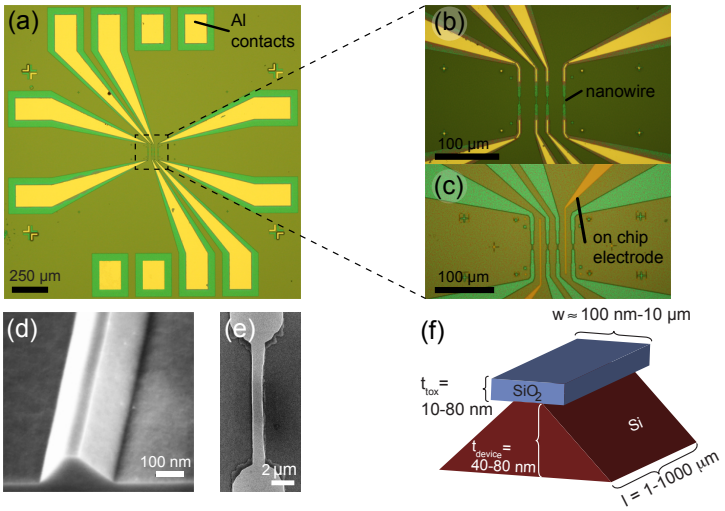


Figure 1.9: Final structure: **(a)** Nanowire FET structure with four wires and connecting leads. Zoom into the nanowire region without **(b)** and with on-chip electrodes **(c)**. **(d)** Geometry of an e-beam fabricated silicon nanowire (SEM picture by courtesy of K. Bedner) and of a UV lithography fabricated nanowire **(e)**. The trapezoidal-shaped nanowire cross section is caused by the anisotropic wet etching of silicon. The height of the wires is given by the device layer thickness **(f)**.

1.4.3 Characterization in ambient environment

To characterize the fabricated FETs under ambient conditions a needle prober station and two different measurement set-ups were used. While all e-beam fabricated nanowire transistors were characterized using a lock-in amplifier (Fig. 1.10a), a set-up with a source meter (DC) was used to characterize nanowires fabricated via UV lithography (Fig. 1.10b). The electrical characterization of the fabricated nanowire FETs was performed in the linear regime at low source-drain voltage V_{sd} between 10 and 100 mV. A DC back-gate voltage V_{bg} was applied via the silicon substrate. An AC voltage (317 Hz) or DC voltage was applied to source and drain contacts. While changing the back-gate voltage the source-drain current I_{sd} was recorded. Measured nanowire FETs showed same behaviour independent of an AC or DC source drain voltage (see appendix A, page 81).

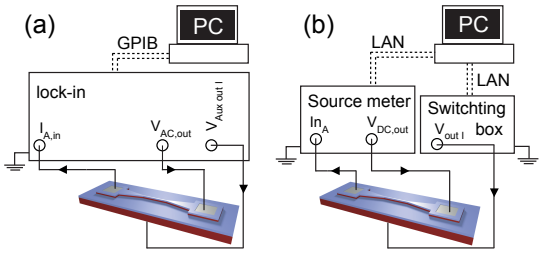


Figure 1.10: Set-ups used for characterization. **(a)** A lock-in was used for AC voltage biasing. **(b)** For DC bias measurements a source-meter was used.

Fig. 1.11 shows the measured transfer characteristics $G(V_{bg})$ of a fabricated nanowire FET for a forward and backward sweep of the gate voltage in linear (black) and logarithmic scale (red). Here the conductance, G, is defined by $G = I_{sd}/V_{sd}$. Appreciable conductance is found both for negative and positive V_{bg}, which shows that the alloyed Al-Si contacts enable both hole and electron transport providing an ambipolar FET. Since the device layer is nominally p-doped, the wires work in accumulation (majority carriers are holes) on the negative V_{bg} side and in inversion on the positive side. The threshold voltages are between -4.5 and $-3.9\,\mathrm{V}$ for the accumulation and $+3.5\,\mathrm{V}$ for the inversion regions, respectively. Here, the threshold voltage is determined by the gate-axis intercept of a linear fit to the $G(V_{bg})$ curve, taken at the inflection point. The transfer characteristics of the fabricated nanowire FETs show an unintentional hysteresis on the accumulation side. This feature has to be avoided since sensing experiments that we will discuss in chapter 2 rely on shifts of the threshold voltage at the mV level range.

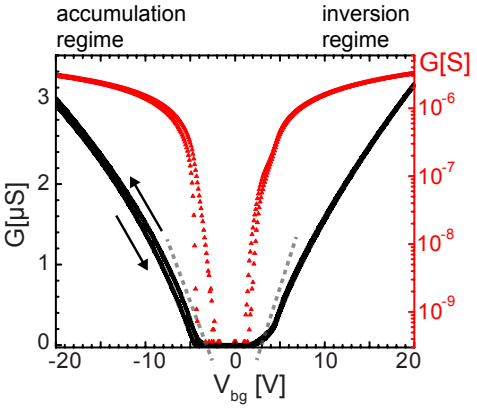


Figure 1.11: Typical transfer characteristic of a fabricated nanowire FET. The electrical conductance G is shown as a function of back-gate voltage V_{bg} measured in ambient in a linear (left axis) and logarithmic (right axis) scale. Both forward (increasing V_{bg}) and backward (decreasing V_{bg}) measurement directions are shown. The threshold voltages V_{th} can be extracted by linear fits (dashed lines, linear scale).

1.4.4 Hysteresis issues

Due to their small dimensions nanowires are very sensitive to surface effects. This however also means that controlling the fabrication process is critical to achieve good reproducibility and stability. The TOX layer as well as the native oxide forming on the side walls may influence the transfer characteristic of the wires substantially [24, 25]. We define here a threshold voltage hysteresis $H_{th} = \mid V_{th\nearrow} - V_{th\searrow} \mid$ to give a value for the hysteresis effect on the extraction of V_{th}. $V_{th\nearrow}$ and $V_{th\searrow}$ denotes the extracted threshold values for the forward and backward sweep directions. Fig. 1.12a shows the conductance of an e-beam fabricated nanowire (l=10 μm, w=100 nm) immediately after fabrication (■) with $H_{th} \approx 3\,\mathrm{V}$, after wet etching of the top oxide layer (●) with $H_{th} \approx 0.5\,\mathrm{V}$ and around one day after the oxide wet etch (△). Here $H_{th} \approx 2.9\,\mathrm{V}$. Three effects can be observed. If hysteresis is present, it is strongly reduced or even lifted once the top oxide and the native oxide were removed [11], showing that surface trapped charges at the oxide level were responsible for the observed hysteresis. The maximal current at large negative back-gate voltages increases significantly, which might also be attributed to the presence of trapped charges leading to a more strongly depleted wire when the oxide is present. Finally, in agreement with the above

argument, the threshold voltage is shifted to less negative voltage values. Here we have to note, that one day after removing the top oxide, the wire characteristics has changed further. If we perform a controlled oxidation (10 min at 100°C) after the top-oxide removal to generate a thin oxide layer of few Angströms (Fig. 1.12b, different sample), then the properties of the wire remain much more stable ($H_{th} \approx 0.42\,\mathrm{V}$), even after two days (△). The hysteresis remains small even after adding the thin protection oxide layer ($H_{th} \approx 0.44\,\mathrm{V}$). We therefore conclude that a controlled thin oxide layer helps stabilizing the nanowires and is important for achieving reproducible devices.

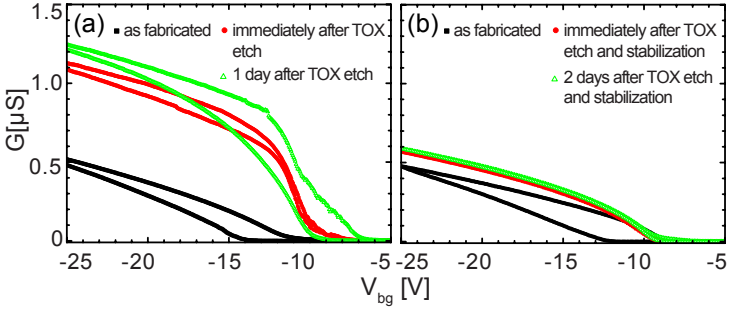


Figure 1.12: **(a)** Transfer characteristics of an e-beam fabricated nanowire FET (l=10 μm, w=100 nm) before and after TOX and native oxide removal. The wire was left without further handling after wet etching. **(b)** A short controlled oxidation was performed directly after wet etching. When hysteresis is present, it is strongly reduced after wet etching. Data derived from two samples.

1.4.5 Reproducibility

A high reproducibility of same nanowire performance has been achieved, when the above results on the stabilization are taken into account. Fig. 1.13a shows the transfer characteristic of a nanowire FET which has been conformally covered with a thin Al_2O_3 atomic layer deposition layer (see chapter 2). The steep transfer characteristic with a low subthreshold swing S of around $80 - 100\,\mathrm{mV/dec}$ indicates a low trap-density and a clean device surface [11, 26]. The ambipolar nanowire-FET shows a small hysteresis between the two gate-voltage sweep directions ($H_{th} \approx 0.4\,\mathrm{V}$). Fig. 1.13b shows the same transfer characteristics for four different NWs on one sample. The curves align almost perfectly on top of each other even with the small hys-

teresis. A high degree of reproducibility has thus been achieved. A slight divergence is only observed at the inversion region which is likely to come from a p-n junction forming at the Al-Si interface [8]. For this reason we will focus in this thesis on the accumulation region of our fabricated devices for following investigations.

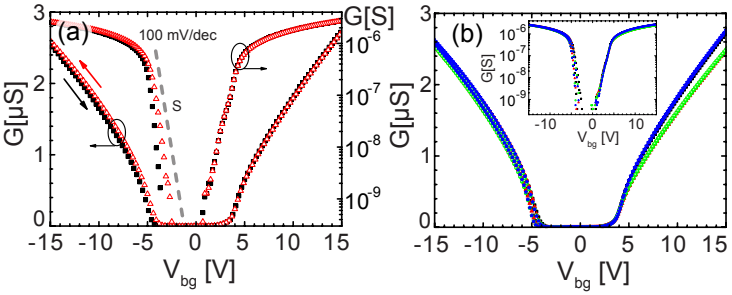


Figure 1.13: **(a)** Transfer characteristic after covering the wire with a thin and conformal Al_2O_3 layer. Both 'forward' (increasing V_{bg}) and 'backwards' (decreasing V_{bg}), demonstrating negligible hysteresis. The subthreshold swing S (dashed line, logarithmic scale) can be extracted to be around 100 mV/dec. **(b)** $G(V_{bg})$ for four different wires demonstrating the excellent reproducibility.

2

Towards Stable Measurement Conditions in Electrolytes

In chapter 1 we showed reproducible characteristics of our top-down fabricated nanowire FETs under ambient conditions. With the focus on chemical and biological sensing, stable functionalities and operations in electrolyte solutions also have to be realized. In this chapter we will discuss the implementation of stable measurements in electrolytic environments for sensor applications. We will introduce and discuss the dual-gate which will be of importance for the next chapters. In addition we will briefly discuss the theory needed to understand the working principle of field-effect transistors in liquid environments[1].

2.1 Introductory remarks

To operate nanowire FETs in liquid environment, the electrical contacts have to be protected from the solvents. For this reason a device was glued onto a chip carrier and bonded (see appendix B for details). Fig. 2.1a shows a final device after a two step sealing process. First, a micron-sized liquid channel was defined in a resist layer by UV lithography. The liquid channel is placed over the nanowires and runs horizontally (Fig. 2.1b). In the second, an insulating epoxy layer was deposited over the contact pads including the

[1] Parts of this work have been published in [27, 28].

bonding wires except for a small opening over the wires area, as depicted in Fig. 2.1a. This configuration allows to protect the contacts and only expose the nanowires to the solution.

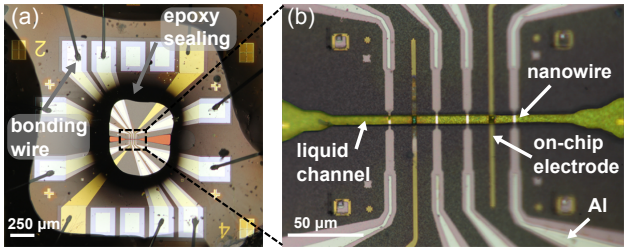


Figure 2.1: **(a)** Optical image of a final device including bonding wires, micron-sized liquid channel and epoxy sealing. **(b)** The SiNWs running vertically with ohmic contacts on the source and drain side made from alloyed aluminum. The micron-sized liquid channel is running horizontally.

2.2 The ion sensitive FET concept

Around the 1960s a number of groups began to work on sensors and transducers built from silicon [29]. This research field expanded enormously and led to many innovative and useful devices. Driven by the demand for chemical, medical and gas sensors at low fabrication cost, researchers turned their focus toward the field-effect transistor (FET). The application of FETs as transducers in (electro-)chemical sensors was first described by Bergveld and coworkers in 1970 [30] with a growing research community ever since [6].

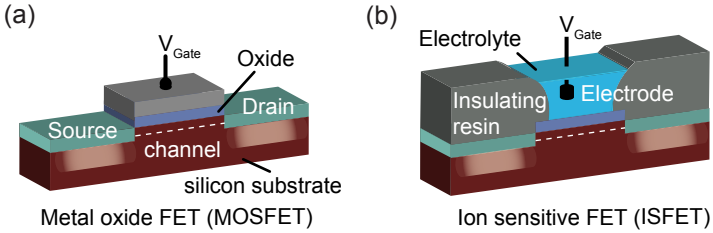


Figure 2.2: **(a)** Schematics of a standard MOSFET and of a ISFET with open gate structure **(b)**.

Such a device uses electrostatic interaction between charged molecules at the surface of the FET and the conductive channel. This leads to an additional gating of the channel. A chemical interaction between the FET and the molecules in the solution is therefore converted into an electrical one. This ion-sensitive FET (ISFET) is in principle a MOSFET with an open gate structure (Fig. 2.2b). The gate metal of the MOSFET is replaced by an electrolyte solution which is contacted by an electrode, immersed into the electrolyte. The gate oxide is in direct contact with the solution. When a ISFET is immersed in an electrolyte, the source drain current can be influenced by changing the ion concentration of a given solution. For a theoretical description of an ISFET, the threshold voltage function of the standard MOSFET needs to be adapted since two new contributions arise: the interfacial potential at the liquid-oxide interface and the constant potential of the electrode E_{ref} relative to vacuum. The metal work function ϕ_m (see page 106) is included in E_{ref}. The interface potential is determined by the sum of the constant solution surface dipole potential, χ [31], and the surface potential ψ_0. ψ_0 results from chemical reactions with the surrounding liquid as we will see in the next chapter. The modified threshold voltage results in [6, 32]

$$V_{th} = E_{ref} - \psi_0 + \chi - \phi_{Si} - \frac{Q_{ox}}{C_g} + 2\psi_B. \tag{2.1}$$

All terms except ψ_0 are constant which shows that the ISFET will be modulated by this term and should hence be sensitivity to agents in the liquid environment.

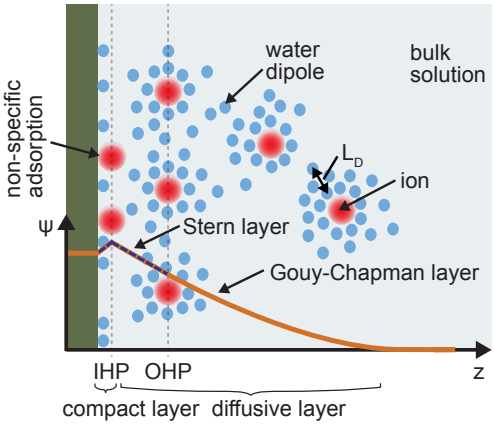
2.3 The electrical double layer in electrolytes

Most sensing experiments, especially biological ones, which are conducted with ISFETs are performed in electrolytic solutions. Electrolytes are the natural environment for most biological systems and are solutions with many dissolved ions (e.g. K^+, Na^+, Cl^-) and since these ions are charged they are able to conduct electrical current [33]. In an electrode-electrolyte system charges will accumulate at the electrode, thus, if a potential is applied to the electrode, ions of opposite charge will be attracted towards its surface and screen the charges of the electrode (Fig. 2.3). A diffusive region of excess ions will be present close to the interface. Since the ions are still surrounded with the polar solvent, they form a relatively thick layer, known as 'Gouy-Chapman double layer', and the charges will give rise to an electrostatic potential drop. The double layer has a characteristic thickness and equals the Debye length (equation C.4 on page 107), which in an electrolyte, is

defined as screening length by

$$L_D = \sqrt{\frac{\epsilon_r \epsilon_0 k_B T}{2Le^2 I}} \tag{2.2}$$

with ϵ_r the relative permittivity of the electrolyte, L being the Avogadro number and I the ionic strength of the electrolyte. I is defined as a function of the concentration all the ions present in the solution $I = \frac{1}{2}\sum c_i z_i^2$ while c_i is the molar concentration of ion i and z_i the charge number of the ion. The potential drop in the double layer and values for typical screening length of monovalent ions such as K^+ or Na^+ are shown in Fig. 2.3.



$c_{sol,KCl}$ [M]	L_D [m]
0.001	~$1 \cdot 10^{-8}$
0.01	~$3 \cdot 10^{-9}$
0.1	~$1 \cdot 10^{-9}$

Figure 2.3: Schematics of a double layer formed in the vicinity of a charged solid state body immersed into an electrolyte. Explanation is given in the text. IHP and OHP denotes the inner and the outer Helmholtz plane. Typical values of the screening lengths for monovalent ions (e.g. K^+ or Cl^-) are given in the table to the right. Adapted from [34].

However the Gouy-Chapman double layer can not fully describe this potential drop. Otto Stern realized that solvated ions cannot approach the surface closer than their ionic radius, known as outer Helmholtz plane (OHP). In this plane, the so called Stern layer, the voltage drops linearly. However there is the possibility of non-specific absorption of ions at the surface forming a compact layer. Here they are able to partially losing their solvation shell. This radius is known as the inner Helmholtz plane (IHP). A more detailed explanation of the double layer and the potential drop can be found in [34, 35].

2.4 Leakage currents in electrolytic environments

A major problem when using FETs as sensors in a solvent containing a concentration $\sim 100\,\mathrm{mM}$, typically the case for bio-sensing, is leakage currents and undesirable electrochemistry at the FET-liquid interface [36, 37]. The latter may change the device and cause degradation with non-reproducible properties.
If a contacted nanowire is immersed in an electrolyte with a liquid-gate electrode, a leakage current, I_{leak}, can flow through two paths, as depicted in Fig. 2.4. The current can flow from the electrolyte through the buried oxide layer into the back-gate contact (Fig. 2.4a). It can also flow from the electrolyte into the source and drain contacts, as it is sketched in Fig. 2.4b.

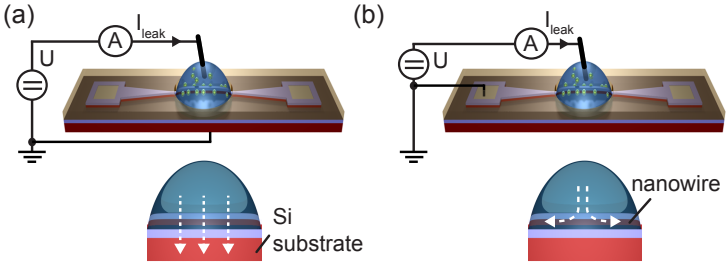


Figure 2.4: Leakage current paths. **(a)** From the liquid gate electrode through the buried oxide layer to the back gate and **(b)** through the wire to the source contact as a function of applied voltage U.

This well known problem can be avoided by covering the surface with a resistant protection layer, which for example can be a stack of alternating Si-oxide and Si-nitride [38]. More recently, atomic-layer deposition (ALD) was introduced successfully for the same purpose [39, 40]. This method has the advantage that it is conformal due to sequential layer-by-layer deposition with high quality layers. In order not to compromise the sensitivity of the FET to analytes adsorbing at the top surface, the protection layer should be as thin as possible. Also here, ALD layers are promising because of the very high degree of control in layer thickness (see appendix B). In Fig. 2.5 we plot typical measured leakage currents for the cases sketched in Fig. 2.4. As electrolyte a pH 8 buffer solution was used[2]. A voltage U between -4 and $4\,\mathrm{V}$ was applied. Although the area exposed to the electrolyte has strongly

[2]Nanowire dimensions: 60 nm top oxide layer, 60 nm thick silicon device layer, a $t_{box} = 150\,\mathrm{nm}$ SiO_2 buried oxide layer and $500\,\mu\mathrm{m}$ thick silicon substrate. The top oxide layer has not been removed from the wire.

been reduced by the definition of the micron-sized liquid channel (shown in Fig. 2.1), a surprisingly large leakage current of 6 nA was measured at $U = 4$ V. Since we used gate voltages up to 10 V, this current relates to a maximum leakage current ≈ 15 nA. The nanowires have a typical linear conductance of 1 μS which has to be measured at a small source-drain bias of, e.g., $V_{sd} = 10$ mV. This relates to a source-drain current of only 10 nA. Hence, without any additional precautions, the leakage current would be comparable to the real source-drain current.

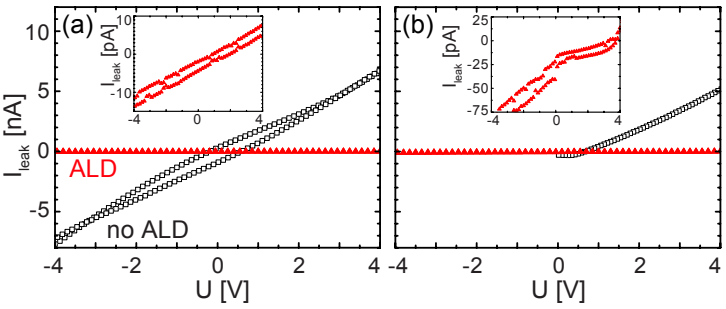


Figure 2.5: Leakage current measured in a buffer solution (Titrisol pH 8) from **(a)** the liquid gate electrode through the buried-oxide layer to the back gate and **(b)** through the wire to the source contact as a function of applied voltage U. The corresponding circuits are sketched in Fig. 2.4. The leakage currents are shown for a device with a fabricated liquid channel but without any further protection (□) and with an additional Al_2O_3 ALD protection layer (▲) on the same scale. 120 layers have been grown in this ALD layer, corresponding to a layer thickness of ≈ 12 nm. In order to see the small residual leakage current with ALD layer a magnified (≈ 100) view is given in the insets.

One solution would be to increase V_{sd}, a strategy that is often seen in the literature, but with the drawback of measuring the conductance in the non-linear transport regime for which a quantitative understanding will be much harder to obtain. Instead, we have solved this problem by a conformal thin coating of a high quality and dense Al_2O_3 ALD layer was deposited over the whole device. As shown in Figs. 2.5a and 2.5b an impressive suppression of leakage current was obtained. The leak current values for both cases are more than two orders of magnitudes smaller (insets in Fig. 2.5). Although leakage is appreciable even with the fabricated liquid channels, the thin layer is enough to suppress the leakage current. The reason for leakage current to flow can be traced back to diffusion of protons from the electrolyte into the device [41]. While it is widely accepted that care should be taken if

measuring in solutions [42], the transport of charges is still not clear. On theory assumes the hydrogen penetration of the surface, which results in complicated hydrogen electrochemistry at the direct vicinity of the oxide surface, in the oxide itself and diffusion into the silicon layers below [43, 44].

As an additional effect coming from the ALD coating, we observe a V_{th} shift toward less negative voltages. Fig. 2.6 shows a $G(V_{bg})$ graph of a nanowire FET after fabrication and deposition of a thin ($\approx$12 nm) Al_2O_3 layer after sealing [41].

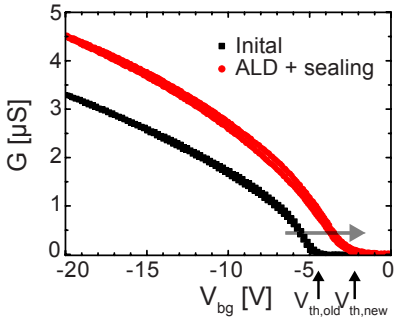


Figure 2.6: Nanowire FET (l=10 μm, w=700 nm) threshold voltage shift after fabrication and after deposition of a thin (in this case $\approx$12 nm) ALD layer. The nanowire FET can be operated at lower voltages.

Taking into account the higher dielectric constant of Al_2O_3 (ε_r=9) compared to SiO_2 ($\varepsilon_r \approx$4) the capacitance per unit area is larger. Charges will be more easily accumulated or depleted in the nanowire resulting in the lower threshold voltage. This well-known effect [45] allows lower FET operational voltages but was not studied in more detail in this thesis.

2.5 Stable characteristics in liquid environments

After having solved the leakage current issue we were able to operate nanowire FETs in liquid environments. A home-built liquid cell allows the integration of a platinum electrode with which a gate potential can be applied (Fig. 2.7a). This electrode acts as liquid gate, V_{lg}, similarly to previous work on carbon nanotube FETs [46]. The potential of the solution, V_{ref}, can be measured using a calomel reference electrode. The liquid cell com-

bines both types of gating, liquid (top)-gating and back-gating, in order to characterize a device.

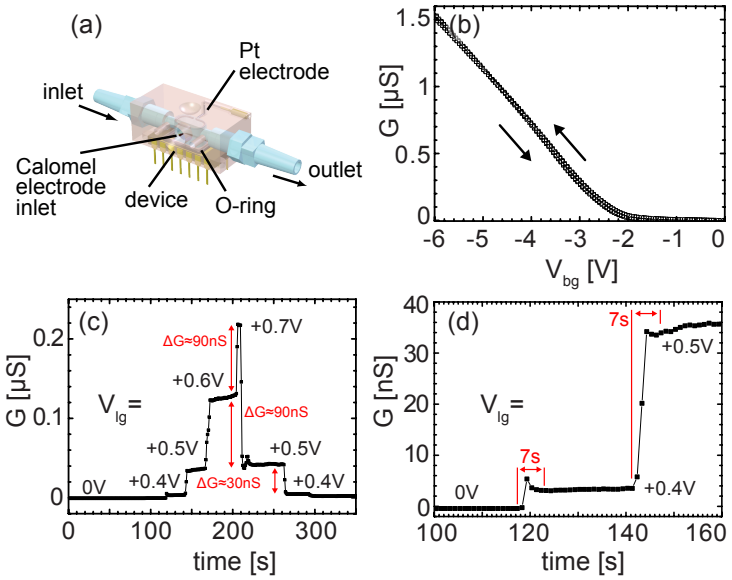


Figure 2.7: **(a)** Drawing of the home-made liquid cell allowing the delivery of liquids and supporting the various electrodes. **(b)** Conductance vs. V_{bg} characteristics of a SiNW FET in a pH 6 buffer solution (V_{lg} floating) for 10 subsequent forward and backward sweeps. **(c)** Conductance response as a function of time while changing the potential of the platinum electrode,V_{lg}, immersed in deionized water (V_{bg} floating). **(d)** shows a magnified cut of (c). The stabilization time after altering the liquid gate as step function (millisecond range) is a few seconds.

Fig. 2.7b shows a typical conductance response in a buffer solution (pH 6) for 10 subsequent back-gate voltage sweeps in forwards and backward direction. V_{lg} was kept floating. Almost no hysteresis is visible, which is an important factor in order to determine the threshold voltage as we will see later on. To demonstrate gating with the liquid gate, a time response of the electrical conductance in de-ionized water while altering V_{lg} is shown in Fig. 2.7c. Here we kept the back-gate contact floating. By sweeping V_{lg} the conductance of the nanowire FET can be tuned as indicated by the vertical red arrows in Fig. 2.7c. The voltage is applied as step function while the change is applied in the millisecond range. Again, we observe

stable operations in liquid environments without an observable drift. The conductance of the FET can be modulated to a constant conductance level. The average stabilization time after altering the liquid gate is a few seconds (Fig. 2.7d) and lies within reported values, e.g. for real-time detection of pH changes [47].

2.6 The dual-gating concept

The geometry of our liquid cell features simultaneous operation of both gates. Figs. 2.8a and 2.8b show a sketch of the dual-gate configuration.

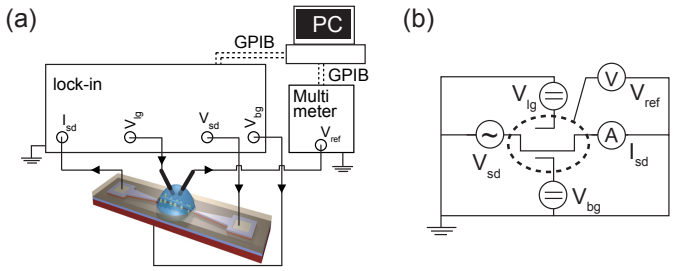


Figure 2.8: **(a)** Sketch of the dual-gate setup applying an AC bias source-drain voltage V_{sd} to the source and drain contact. The back-gate voltage V_{bg} is applied through the Si substrate and the liquid gate V_{lg} is applied via a Pt gate immersed into the solution. The potential of the liquid V_{ref} is simultaneously measured by a calomel reference electrode. The equivalent circuit is shown in **(b)**.

The result is shown in the dual-gate diagram of Fig. 2.9a, where the conductance is represented in a colour-coded contour plot as a function of the applied gate voltages V_{bg} and V_{lg}. As an electrolyte, a 1 mM KCl solution in de-ionized water was used.

For positive voltages at both gates, the device is in the n-regime, while for negative voltages it is in the p-regime as depicted by the letters 'n' and 'p' in Fig. 2.9. In our geometry the leads are semiconducting with the same doping level as the nanowires. Hence they will also be gated by the back-gate. For $V_{bg} > 0$ and $V_{lg} < 0$ the nanowire is driven in the p-regime by the electrolyte-gate whereas the leads – insulated from the liquid – are driven in the n-regime by the back-gate. In this case, the device forms an npn-junction. For $V_{bg} < 0$ and $V_{lg} > 0$, we obtain a pnp-junction. In both cases the current is suppressed. At $V_{bg} \approx$-3 V and $\approx$6 V a pronounced kink is

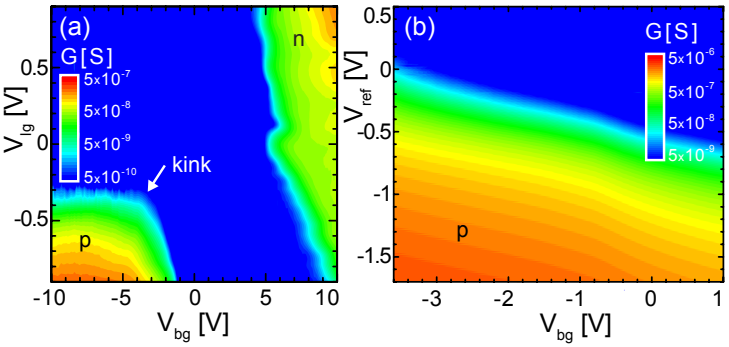


Figure 2.9: Dual-gate diagram of two different devices. **(a)** Contour plot of nanowire conductance G (colour-coded) versus back-gate V_{bg} and applied liquid gate V_{lg} in a 1mM KCl solution in de-ionized water (dimensions: length = 1 μm, width = 100 nm). The letter 'p' denotes the accumulation regime while the letter 'n' denotes the inversion regime. A pronounced kink is visible. **(b)** Dual-gate conductance plot of NW conductance G versus back-gate V_{bg} and measured potential of the solution V_{ref} in pH 5 buffer solution. The contacts are highly p-doped (dimensions: length = 10 μm, width = 1 μm) which blocks the n-regime.

visible, an effect due to influence of the contact leads. To remove this effect, metallic or highly doped contact leads can be used. Fig. 2.9b shows a 2d-map of a nanowire FET with highly doped contacts (p-doped $> 10^{19} cm^{-3}$) plotted against the measured liquid potential V_{ref}. The kink (cut-off region) observed using low doped semiconducting contact leads disappears. In contrast the n-regime is suppressed since highly p-doped contacts block electron transport.

2.7 Contact leads influences

To prove that the kink, cut-off region, in the 2d plot is actually caused by the contact leads and is not intrinsic to the nanowire, we conducted an experiment recording 2d-conductance maps for different ion concentrations, which affects the capacitance from the liquid to the nanowire (liquid capacitance) [48]. In contrast, the capacitance from the liquid to the contact leads is much lower and determined by the polymer layer that covers and protects the contact leads, forming a liquid channel over the nanowire. With increasing ion concentration the capacitance of the double layer at the interface of the top surface of the nanowire and the liquid *increases*. This changes

the capacitance ratio between back-gate and liquid gate, which one would expect to *decrease* with increasing ion concentration.
The 2d conductance plots in Fig. 2.10 were measured in a dilution series in DPBS (Dulbeccos Phosphate Buffered Saline) solution. From top-left to bottom-right the concentrations are 10^{-4}, 10^{-3}, 10^{-2}, and 0.1 M, respectively. In the left part of the kink ($V_{bg} < -5\,\mathrm{V}$), the slope gradually lowers when the ion concentration is increased. This is exactly what we expect, since the magnitude of the slope is given by C_{bg}/C_{lg}, where C_{bg} denotes the back-gate and C_{lg} the liquid-gate capacitance. In contrast, in the right part of the kink ($V_{bg} > -3\,\mathrm{V}$) the slope is not changed at all. This proves that only the left part is in close contact with the electrolyte. Hence, in the left part of the kink, the nanowire is depleted. In contrast, the contact leads are depleted in the right part of the kink while the nanowire itself is still in accumulation. In the left part the slope, and hence the capacitance ratio C_{bg}/C_{lg}, changes by approximately one order of magnitude for a concentration change of three orders of magnitudes. If the liquid capacitance was solely determined by the double-layer, one would expect a dependence $C_{lg} \propto \sqrt{c_{ion}}$, where c_{ion} denotes the ion concentration. The somewhat reduced change points to the importance of all additional capacitances, such as the top-oxide capacitance, which will be discussed in more detail in the next chapter.

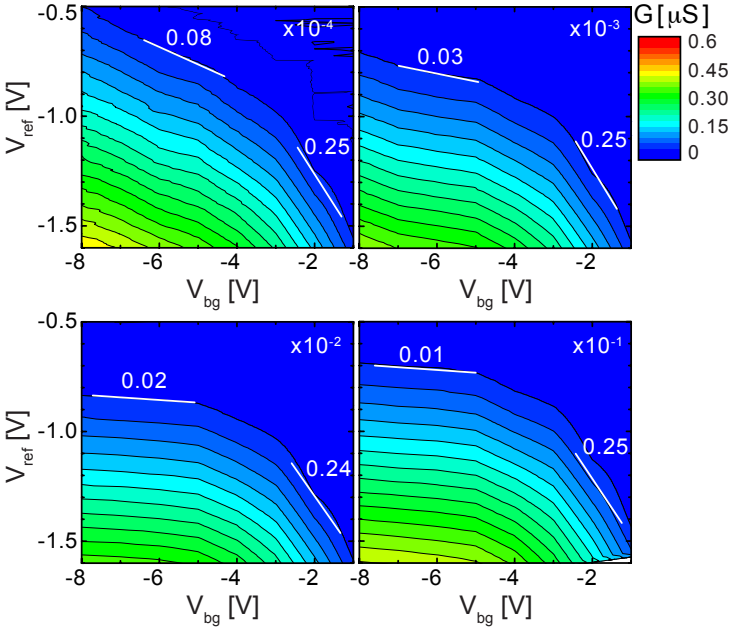


Figure 2.10: Two-dimensional conductance maps measured in a DPBS (Dulbeccos Phosphate Buffered Saline) buffer at various molar concentration between 10^{-4} (top left) to 0.1 (bottom right). The ion concentration has a pronounced effect on the left region ($-8\,V < V_{bg} < -4\,V$), but does not affect the right one ($-3\,V < V_{bg} < -1\,V$). The nanowire is 100 nm wide and 1 μm long. This sample did not have yet an ALD layer incorporated. The layer thicknesses are from top to bottom $t_{tox} \sim 70$, $t \sim 70$ and $t_{box} = 150$ nm for the top-oxide, nanowire and buried oxide layers, respectively. A silver wire acted as quasi-reference electrode. The white lines indicate the magnitude of the slope at the respective contour lines. They correspond to two different ratios of the coupling capacitance between the back- and liquid-gate.

2.8 Summary

In conclusion, we achieved reproducible and stable operations in liquid environments without observable drift. Although the devices are protected up to a small micrometer-scaled liquid channel, we explicitly showed that leakage currents can be appreciable in an electrolyte. However, the leakage currents can sufficiently be suppressed with a thin Al_2O_3 ALD layer. Both V_{bg} and V_{lg} allow the positioning of the nanowire at a stable "working point". The short settling time is promising for real-time sensing experiments.

3

Accessing (pH-) Sensing with Nanowire FETs

In the previous chapter we showed necessary steps to achieve stable nanowire FET operations in electrolytic environments. In this chapter we will discuss sensing capabilities with the wire. We studied the nanowires as ISFETs and conducted pH sensing experiments using the dual-gate concept introduced before[1].

3.1 Nanowire FETs as ISFET sensors

The idea of gating the channel of an FET using the electrostatic interaction between charged molecules adsorbed on the surface was demonstrated for the first time by measuring the proton concentration (pH) of an electrolyte [6, 30]. The concept of the ISFET has recently been applied to nano-scale devices such as carbon nanotubes [17, 46, 49, 50] and nanowire FETs [19, 21, 51, 52]. Due to the the large surface-to-volume ratio, a high sensitivity can be expected for nanowire FETs [53]. This has allowed the detection of analytes with dilutions in the femto-molar range [21, 54] and to approach the single-molecule limit through the detection of a few proteins [55]. Decreasing the size of the sensing device reduces the electrostatic capacitances, which in addition provides shorter response times [47]. To provide a reliable diagnosis with selectivity in a real-life application, multi-functionalized sensors are

[1] Parts of this work have been published in [28].

essential. One therefore strives to integrate nanowire FETs into wafer-scale arrays by adding on-chip micro-fluidics [56]. This allows for correlation measurements if differently functionalized sensors are used [57]. However, the operation of single nanowire FETs in liquids and their sensing capabilities are far from being understood today and in order to achieve optimal working conditions, an improved understanding of the basic sensing mechanism is required [58, 59, 60, 61]. The large knowledge in pH-sensing using ISFET can be used to benchmark nanowire FETs.

3.1.1 The oxide-electrolyte interface

For an ISFET with an open gate structure, ions can approach the surface, the interface of the FET and the electrolyte. The ions in the solution can undergo a reaction with the surface. In this thesis, Al_2O_3 is used as the interfacial layer. In case of pH, the oxide surface of the FET channel can adopt a positive or negative surface charge. Depending on the sign, this will either increase or decrease the channel conductance. It is well-known that the outermost surface of an oxide or an oxide film contains a layer of amphoteric hydroxyl groups (-MOH), M refers to a surface site occupied by a metal cation) [62]. In case of SiO_2 or Al_2O_3, Si-OH respectively Al-OH groups. In aqueous solution, these groups interact with protons in the bulk solution, H_B^+, first introduced by Yates et al. [63] known as site-binding model.

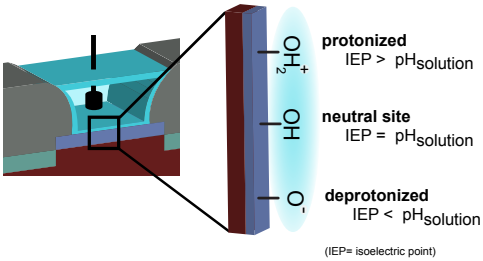


Figure 3.1: Sketch of an ISFET oxide-liquid interface.

Depending on the isoelectric point (IEP) of the surface, the point where the surface is neutral, and the pH of the solution (Fig. 3.1), these hydroxyl groups can be either neutral, protonized (positively charged) or deprotonized (negatively charged) due to dissociation of the surface hydroxyl group [64, 65]. By donating or accepting a proton from the bulk solution the (-OH) groups are able to undergo a reaction, which can be summarized as

$$MOH \rightleftharpoons MO^- + H_B^+$$
$$MOH_2^+ \rightleftharpoons MOH + H_B^+. \tag{3.1}$$

These reactions will charge the FET's surface more positively or negatively, acting as an additional gate and influencing the conducting channel beneath. Using the Boltzmann equation, the activity of the protons at the direct vicinity of the FET's oxide surface can be related to the bulk protons activity [6]

$$a_{H_S^+} = a_{H_B^+} e^{\frac{-e\psi_0}{k_B T}} \quad \text{or} \quad \Delta\psi_0 = 2.3\frac{k_B T}{e}(\Delta pH_S^+ - \Delta pH_B^+). \tag{3.2}$$

Here $a_{H_S^+}$ and $a_{H_B^+}$ denote the activity of protons at the surface and the bulk, while pH_S^+ and pH_B^+ denote the pH at the surface and the bulk solution. ψ_0 is the potential change at the surface between the electrolyte-oxide interface, introduced in chapter 2. The activity is a measure of the effective concentration of a given molecule defined as $a_i = e^{\mu_i - \mu_i^{\ominus}/RT}$. μ_i is the chemical potential of the molecule at the desired condition while $\mu_i^{\ominus}$ defines the chemical potential in the chosen standard state. R denotes the gas constant. We refer to appendix C, page 109, for a more detailed discussion. Since we have used a p-type Si device layer and operate the FET in accumulation, adding negative surface charge increases the carrier concentration in the channel, whereas adding positive charge will tend to deplete the channel. In the ISFET literature this change in the electrical conductance is usually expressed as a shift in the conductance versus gate-voltage (either back-gate or liquid-gate) curve, typically measured as a threshold shift ΔV_{th}. In an ideal ISFET the maximum threshold shift is determined by equation (3.2) which predicts a maximum shift of 59.5 mV/pH at room temperature (300 K). This maximum value can only be reached if pH_S^+ is constant while pH_B^+ changes. This will be the case, if the oxide surface are able to buffer small changes in the proton concentration at its direct vicinity.

3.2 Experimental remarks

The nanowire FETs used for the following experiment consists from top to bottom of a 60 nm top oxide layer, a 60 nm thick silicon device layer, a $t_{box} = 150$ nm SiO_2 buried oxide layer and the 500 μm thick silicon substrate. The top oxide layer has not been removed from the nanowire [27].

The whole device was conformably covered by a high quality thin 12 nm Al_2O_3 ALD layer (Fig. 3.2a). Viewed in the lateral direction, the etched nanowire widens up and evolves into connecting source and drain leads of width 5 μm. It is important to realize that the ohmic contacts start $\approx 20\,\mu$m away from the wires (Fig. 3.2b). Hence, there is an additional lead resistance which we estimate to be half the nanowire resistance for a uniform carrier density. This fact is also emphasized in the schematics of Fig. 3.2c. We used the dual-gate approach introduced in the previous chapter [27, 66, 67]. While the back-gate voltage V_{bg} is applied to the Si substrate, the liquid gate voltage V_{lg} is applied to a platinum electrode immersed into the solution. At the same time, the liquid potential V_{ref} is measured by a calomel reference electrode. For the standard pH solutions we find a linear relation between the measured liquid potential V_{ref} and V_{lg} with a slope close to one [48]. This shows that there are no spurious electrochemical reactions taking place at the Pt electrode for these electrolytes. The liquid potential has to be recorded in order to ensure comparable measurements in electrolytes [68, 69]. The electrical characterization of the fabricated nanowire FETs was performed at low source-drain voltage between 10 and 100 mV using a lock-in amplifier (frequency 317 Hz) to measure the source-drain current I_{sd}.

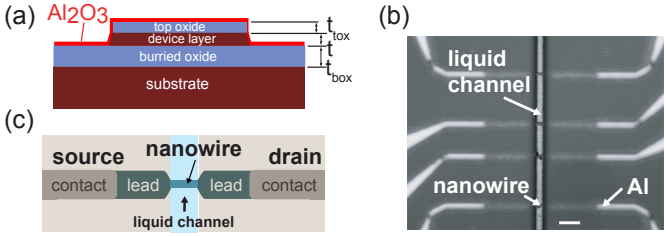


Figure 3.2: **(a)** Schematics showing a nanowire in cross section. The layer thicknesses are from top to bottom $t_{Al2O3} \sim 10$, $t_{tox} \sim 60$, $t \sim 60$ and $t_{box} = 150$ nm for the Al_2O_3, top-oxide, nanowire and buried oxide layers, respectively. The nanowires are 700 nm wide and 10 μm long. **(b)** Optical image of four wires running horizontally (scale bar = 10 μm) with ohmic contacts on the source and drain side made from alloyed aluminum. The micron-sized liquid channel is running vertically. **(c)** shows schematically the lateral structure with the nanowires in the center evolving into wider contact leads into which Al is alloyed at a distance of $\approx 20\,\mu$m away from the wire.

3.3 pH sensing

To demonstrate sensing we used the wires as ISFETs performing pH measurements in different electrolyte buffer solutions. This is well established in the current literature, see for example [19, 21, 60]. Fig. 3.3 shows 2d-conductance (G) maps measured at different pH buffer solutions as a function of both V_{bg} (horizontal axis) and V_{ref} (vertical axis). The lines of constant G-values evolve from a small slope $s = \partial V_{ref}/\partial V_{bg}|_{(G=const)}$ in the upper part ($V_{ref} > 0\,\mathrm{V}$) to a large in the lower part ($V_{ref} < 0\,\mathrm{V}$). This cross-over leads to a pronounced kink at the border from accumulation to depletion at $(V_{bg}, V_{ref}) \approx (-4, 0)\,\mathrm{V}$. At this border the slopes (white lines, Fig. 3.3 bottom right) are $|s| = 0.43$ for ($V_{ref} \approx 0.3\,\mathrm{V}$) and 7.25 for ($V_{ref} \approx -0.8\,\mathrm{V}$), respectively. This dependence can be understood by considering the different gating capacitances as we explained previously and will outline in the following in more detail.

Gating changes the total charge contribution in the wire. This includes the mobile minority and majority carriers as well as ionized dopants. Since the two gates act from different sides, one from above and the other from below, one may first ask whether the charge is constant throughout the thickness t of the nanowire or not. The relevant length scale is the Thomas-Fermi screening length, λ, which for classical Boltzmann statistics is $\lambda = \sqrt{\epsilon_{Si}\epsilon_0 k_B T/e\rho}$ (appendix C). Here, $\epsilon_{Si} = 12$ is the relative dielectric constant of Si and ρ the relevant mobile carrier density. A boron-doped wafer with a resistivity of $10 - 20\,\Omega\mathrm{cm}$ has a doping concentration of $N = 10^{15}\,\mathrm{cm}^{-3}$ [8]. Since this is close to the intrinsic carrier concentration at room temperature, it is a good estimate for ρ in the depletion region. Using these numbers, we obtain $\lambda = 130\,\mathrm{nm}$, which is substantially larger than the thickness $t = 60\,\mathrm{nm}$ of the device layer. Unlike the conclusions of Elibol *et al.* [66] we find that gating is uniform throughout the thickness of the wire. It therefore does not matter, whether gating is applied from the back or from the top side.

However, with regard to the lateral geometry, the two gates are not identical. Whereas the back-gate is always at the same distance to the device layer, this is different for the liquid gate. Due to the liquid channel defined in the resist layer on top of the device, the coupling capacitance from the liquid to the wire must be different than to the attached source and drain leads, see Fig. 3.2c. Hence, the contact resistance in the leads is differently affected by the gates than the resistance of the wire. To quantify this, we look back to the lines of constant G in Fig. 3.3. Assuming that G is solely determined by the nanowire, a constant G value must correspond to a constant charge state in the NW. Since the induced gate charge Q in the wire is proportional

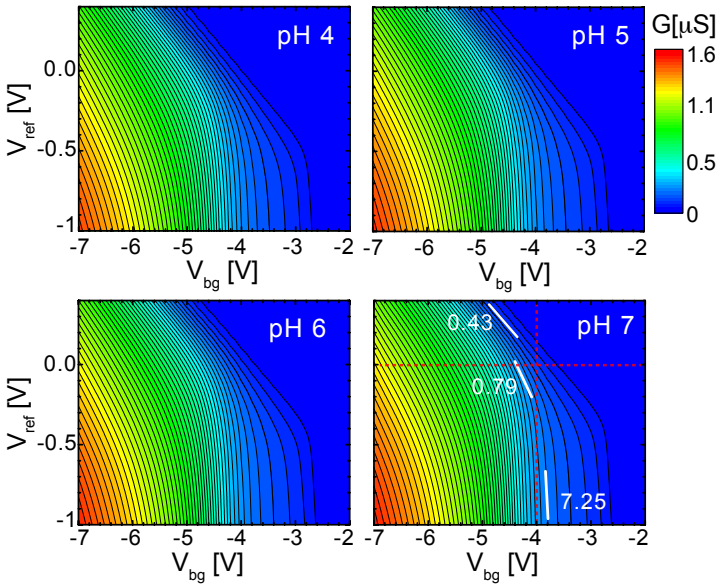


Figure 3.3: Two-dimensional conductance (G) map for different pH buffer solutions. G is displayed together with contour lines as a function of the back-gate voltage V_{bg} and the measured liquid potential V_{ref}. In the bottom right plot dashed lines highlight the parameter ranges that were used in the cuts in Fig. 3.4. The white lines in the lower right graph indicate the the slope at the respective contour lines. They correspond to different ratios of the coupling capacitance between the back- and liquid-gate.

to $C_{bg}V_{bg}$ for the back-gate and to $C_{lg}V_{ref}$ for the liquid gate, the slope s is given by $s = -C_{bg}/C_{lg}$, where C_{bg} and C_{lg} denote the back-gate and liquid-gate capacitances acting on the nanowire. The liquid gate-capacitance is the series connection of the electrolyte-solid interface capacitance (double layer capacitance) and the geometrical capacitances of the Al_2O_3 and the Si top-oxide layer. Because the latter is the smallest, C_{lg} can be approximated by this one. With the device cross-section in mind (Fig. 3.2a), this number is predicted to be equal to $s \approx -t_{tox}/t_{box} \approx -0.4$, in very good agreement to the value of 0.43 measured in the upper part of Fig. 3.3d. It is clear that the large slope of 7.25 in the lower right part of the G-map can be assigned to the gating of the connecting leads, because for those the gating efficiency from the liquid is drastically reduced due to the resist layer lying over the source and drain leads.

In Fig. 3.4 we show cuts through the 2d-G-maps (dashed red lines, Fig. 3.3d) for a constant back-gate voltage V_{bg} of $-4\,\mathrm{V}$ in (a) and for a constant liquid potential V_{ref} of $0\,\mathrm{V}$ in (b). Both sets of curves display clear shifts. The curves shift to more positive gate values (increase in conductance) for increasing pH (decreasing proton concentration). This is the expected dependence for an oxide surface exposing hydroxyl groups to the liquid. The change in surface charge density caused by a pH change is described by the site-binding model [63], which takes into account that (-OH) groups can be protonated or deprotonated. This model predicts an approximate linear relation between the surface charge density and the proton concentration. Since the surface charge acts as an additional gate, the p-doped NW-FET is depleted if the proton concentration is increased (pH decreased).

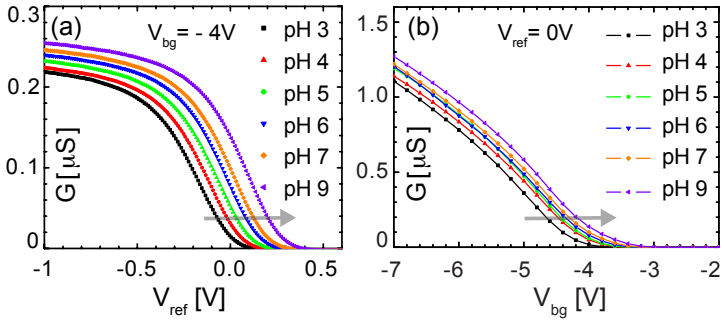


Figure 3.4: Effect of pH change on the transfer characteristics measured as a function of V_{ref} and V_{bg}. In **(a)** the effect is shown by the set of $G(V_{ref})$ curves for a fixed V_{bg} of $-4\,\mathrm{V}$ and different pH values, whereas in **(b)** it is shown by the set of $G(V_{bg})$ curves for a fixed V_{ref} of $0\,\mathrm{V}$. For increasing pH values the conductance curves shift to more positive gate values.

First, we deduce the pH induced threshold voltages V_{th} at a fixed back-gate voltage V_{bg} when sweeping the liquid potential V_{lg}. This is shown in Fig. 3.5a for $V_{bg} = -3\,\mathrm{V}$ ($\triangle$), $-4\,\mathrm{V}$ ($\Diamond$), and $-5\,\mathrm{V}$ ($\square$). For the sensitivity as measured by the change ΔV_{th} of the threshold voltage relative to the pH change we derive values of $\sim 45\,\mathrm{mV/pH}$ for this device. Other devices show values up to $59\,\mathrm{mV/pH}$ (Fig. A.5, appendix A). The deduced sensitivity is in good agreement with reported values for Al_2O_3 layers terminating the surface to the liquid interface [40]. It is higher than values reported for SiO_2 surface layers [6, 19, 56, 60], which is due to higher buffer capacity of the Al_2O_3 surface. In classical thermodynamics at relatively low

concentration, chemical potentials depend on the logarithm of the concentration c (eq. 3.2). If we are dealing with charged species and an interface in equilibrium (without a current flow), the constant electro-chemical potential converts the chemical potential difference between the liquid and solid phase into an electro-static potential difference $\Delta\psi_0 = (2.3k_BT/e)\log(c)$. Here, T is the absolute temperature and $2.3 = log(e)$. The prefactor is the Nernst value which is equal to 59.5 mV/pH at room temperature, indicated in Fig. 3.5 by the dotted line. It is usually assumed that the potential step $\Delta\psi_0$ determines the maximum possible threshold shift in an ion-sensitive FET [6].

Next, we deduce the pH induced threshold voltages V_{th} at a fixed liquid potential V_{ref} when sweeping the back-gate voltage V_{bg}. This is shown in Fig. 3.5b for $V_{ref} = -0.8\,\mathrm{V}$, (•), 0 V (▼), 0.3 V (★), and 0.5 V (∗). Surprisingly, the sensitivity can vary over orders of magnitudes with very small values of only a few mV/pH to values of 220 mV/pH that greatly exceed the Nernst 'limit'. The low values can readily be explained, as they were measured for small liquid potentials where the total conductance of the device is limited by the leads and not by the wire.

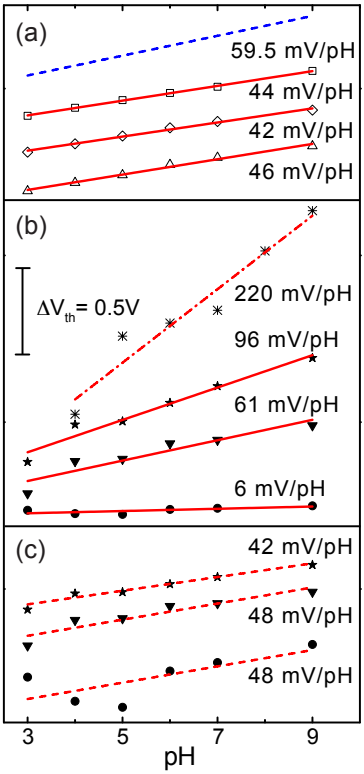


Figure 3.5: Measured threshold voltages V_{th} in different pH buffers measured in **(a)** for a fixed back-gate voltage from bottom to top $V_{bg} = -3$ (△), -4 (◇), and $-5\,\mathrm{V}$ (□) and in **(b)** for a fixed liquid potential of $V_{ref} = -0.8$ (●), 0 (▼), $0.3\,\mathrm{V}$, (★), and $= 0.5\,\mathrm{V}$ (∗). The latter measurements, summarized with the dash-dotted line, is from a different device (appendix A). The slopes of the fits define the sensitivity. As a reference, the dashed line in (a) gives the Nernst value of $59.5\,\mathrm{mV/pH}$ at room temperature. The sensitivities greatly scatter depending on the working point. In measurements against V_{bg}, the sensitivity can even assume values larger than the Nernst limit. **(c)** Taking into account the gate coupling ratios C_{lg}/C_{bg} (highlighted in Fig. 3.3 by white lines), sensitivity values between 42 and $48\,\mathrm{mV/pH}$ are obtained, consistent with the ones shown in (a).

3.4 Explanation of the high sensitivities

We can analyse our findings by using the effective capacitance network. At equilibrium when no or only a small source-drain voltage is applied, the charge states are defined by the capacitors shown in Fig. 3.6. The various capacitances are the double-layer capacitance C_{dl} at the electrolyte-solid interface, the capacitance of the thin oxide layer C_{ox} on top of the nano-wire, the back-gate capacitance C_{bg}, an effective contact capacitance C_c to the source and drain contacts, and the internal electrochemical capacitance C_{NW}, also sometimes referred to as the quantum capacitance [70, 71]. The latter appears because of the relatively low density-of-states in a semiconductor, resulting in an appreciable change of the internal chemical potential if the charge Q in the nano-wire is altered. Because the nano-wire can exchange charge carriers with the source and drain contacts, its electrochemical potential is maintained constant. As a consequence, the change in chemical potential is cast into an electrostatic potential change of equal magnitude. For a one-dimensional system, the contact capacitance C_c is expected to be $<< C_{NW}$ and can therefore be neglected.

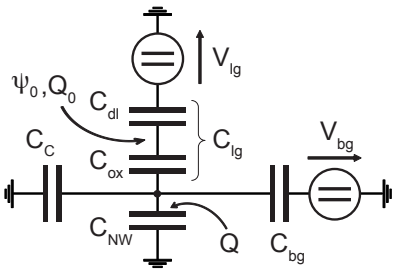


Figure 3.6: At equilibrium when no or only a small source-drain voltage is applied, the charge states are defined by the capacitors shown in this schematics. C_{bg} denotes the back-gate and C_{lg} the liquid-gate capacitor. The latter is composed of the series circuit of an electrolyte double-layer capacitance C_{dl} and the oxide capacitance C_{ox} defined by the top oxide. The nano-wire is located at the central node and its own charging characteristics is summarized with C_{NW}. Q denotes the screening charge in the wire, Q_0 and ψ_0 denote the charge and potential at the solid-liquid interface above the nanowire. Finally, C_c is the contact capacitance between the NW and source and drain contacts.

According to the well-known Bergveld model for ISFET operation [6], the threshold shift ΔV_{th} in the conductance versus liquid-gate voltage V_{lg} caused by a change in the proton concentration in the bulk electrolyte ΔpH closely follows Nernst's equation. More specifically,

$$\Delta V_{th} = -2.3\frac{k_B T}{e} \cdot \alpha \Delta \mathrm{pH}, \tag{3.3}$$

where α is the dimensionless sensitivity parameter $\alpha = (C_{dl}/C_s + 1)^{-1}$ with C_s denoting the surface buffer capacitance determined by the density of active (-OH) groups on the surface (see appendix C for more details). Obviously, α may vary between 0 and 1 and obviously $\alpha \leq 1$. In the derivation of this formula [6], C_{dl} has implicitly been assumed to be much larger than C_{ox}, C_{NW} and C_{bg}. Under these assumptions, one can therefore state that the liquid-gate shift is always smaller than $2.3k_BT/e = 59.5\,\mathrm{mV/pH}$ at room temperature. The ISFET sensitivity approaches the Nernst limit with $\alpha \sim 1$ if $C_s \gg C_{dl}$.
If, on the other hand, the pH-dependent shifts in the conductance curves are measured relative to the back-gate, values that differ from the Nernst limit are possible. To obtain the respective shifts δV_{bg} per pH change, we calculate the responses $\delta Q/\delta V_{bg}$ and relate it to $\delta Q/\delta V_{lg}$ (appendix C, page 113). We obtain

$$\frac{\delta V_{lg}}{\delta V_{bg}} = \frac{C_{bg}}{C_{lg}}, \tag{3.4}$$

where C_{lg} denotes the liquid-gate capacitance given by the series connection of C_{dl} with C_{ox}. For typical high-ion concentrations as being used in buffer solutions $C_{dl} >> C_{ox}$, so that this voltage divider is given in practice by the ratio C_{ox}/C_{bg}. Depending on this ratio, the pH-induced back-gate voltage shift can be reduced or enhanced. It is enhanced if the $C_{bg} < C_{ox}$ which can result into a signal with an *apparent* sensitivity exceeding the Nernst limit.
Since the capacitance ratio between the back-gate and liquid-gate can be measured, we can check this model. As emphasized before, the ratio is given by the slope s in the 2d conductance map shown in Fig. 3.3d where it is indicated by the white slope. If capacitance ratios close to depletion are used, the extracted sensitivity values measured against V_{bg} can be converted into corresponding values measured against V_{lg} using equation (3.4). The result of this procedure is shown in Fig. 3.5c for the three data sets that show sensitivities of 6, 61, and 96 mV/pH if measured against V_{bg}. After multiplication with the capacitance ratio sensitivities between 42 and 48 mV/pH are obtained. This is consistent with the threshold shifts measured against the liquid gate, which lead to values between 42 and 46 mV/pH.

3.5 Time dependent sensing

In this section we will discuss time-dependent pH sensing experiments. We have conducted such experiments with the same nanowire FET presented in the previous section (page 36). These measurements are comparable with experiments reported in the literature [21, 56, 60].

Figs. 3.7a and 3.7b show the time-response of the electrical conductance of the nanowire at different working points while changing the pH values from pH 3 up to pH 5.

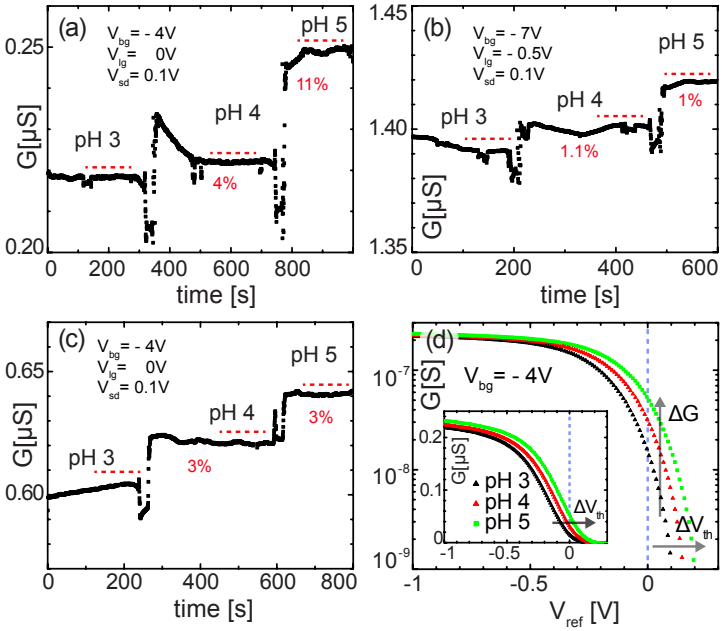


Figure 3.7: Conductance response of a SiNW FET as a function of time while changing of solution's pH, from pH 3 to pH 5. The working point was set near the subthreshold regime in **(a)** and the linear regime in **(b)**. **(c)** Conductance response for a different SiNW FET as function of time in the linear regime. Red numbers correspond to the conductance ratio $\Delta G/G_0$. **(d)** Comparison of the different analysing methods. The blue line indicates the working point used in (a).

The working point was set near the subthreshold regime (Fig. 3.7a) and

the linear regime (Fig. 3.7b). Fig. 3.7c shows the time-response of G in the linear regime for a nanowire FET on a different device but with the same specifications. The large fluctuations between two pH values are due to manually exchanging flasks containing the pH buffer solutions while recording the current.
The most pronounced effect when increasing the pH value is the conductance increase. At higher pH value the wire is in a more conductive state. In contrast to our previous analysis method where the sensitivity has been derived by the threshold voltage shifts ΔV_{th} (inset Fig. 3.7d), here we have to define a different device sensitivity. Here, the sensitivity, Z, is given by the change in the wire conductance (ΔG) induced by the pH change. This value is normalized by an initial device conductance (G_0), e.g. G at pH 3, at constant source-drain voltage [72]

$$Z = \frac{G - G_0}{G_0} \cdot 100\% = \frac{\Delta G}{G_0} \cdot 100\%. \tag{3.5}$$

The red lines in Fig. 3.7 are guides to the eye and denote the value of G_0 used to calculate Z. While for working points in the linear regime the sensitivity remains constant (Figs. 3.7b and 3.7c), it changes dramatically for a working point next to the subthreshold regime (Fig. 3.7a). This large change is known in the literature [60]. In this region the current increases exponentially (equation (1.5)). Hence using Z, we will obtain different values depending on the current level in the subthreshold regime (indicated by the vertical arrow in Fig. 3.7d). In contrast, a constant voltage shift is obtained using the ΔV_{th} method, independent of the current (conductance) level as indicated by the horizontal arrows in Fig. 3.7d in the linear and the subthreshold regime.

3.6 Summary

In summary, we showed that a nanowire FET can be used as a sensing device. We demonstrated that we can measure pH shifts either by sweeping the back-gate voltage or the liquid potential. A small back-gate capacitance can even amplify the sensitivity to pH changes when threshold voltage shifts are measured relative to the back-gate with apparent sensitivities that can exceed the Nernst limit. If one takes the proper capacitance ratio into account, consistent values are obtained for both cases. Our observations are important for sensing experiments in physiological experiments where the liquid potential has to be controlled separately and maintained constant during the experiment. Similar experiments recently conducted on different systems (organic and ZnO FETs) confirm our findings [73, 74]. We com-

pared the two models which are used in the common literature to analyse the sensitivity of nano-scaled sensors.

4

Impact of different Salt Concentrations

In this chapter we will expand the application of our nanowire FETs as ion-sensitive sensors. Since pH buffer solutions contain several different salts (e.g. KH_2PO_4 and Na_2HPO_4) at different concentrations as buffering agents an important aspect is to study the effects of different salts. For this reason we investigated the response of the nanowire FET to different types of ions (such as K^+,Cl^-, Mg^{2+}, Na^+ and SO_4^{2-}) and concentrations dissolved in de-ionized water while leaving the proton concentration (pH) constant. For the following experiments the FET has been chosen to have larger dimensions to ensure homogeneous gating conditions.

4.1 Monovalent and divalent ions

In the previous chapter we concluded that, in particular, nanowire FETs show good results for the detection of pH values. We showed that an oxide surface with its hydroxyl groups is sensitive to a change of the proton concentration in the bulk solution. Besides proton concentration detection, there have been attempts to detect other kinds of ions using nanowire FETs with an oxide interface [47, 75, 76], however, with diverging results. Nikolaides et al. [75] and Park et al. [47] reported on a weak non-linear change of the FET resistance upon changing the ion concentration of a KCl and respectively of a NaCl solution. In contrast, Clément et al. [76] reported a full linear Nernstian response of about 60 mV/dec to NaCl. To resolve the

inconsistency in the literature reporting on different sensitivities to (monovalent) ions, e.g., K^+ or Cl^-, we measured the transfer characteristics of our nanowire FETs at different KCl concentrations dissolved in de-ionized (DI) water. The pH values of all solutions were monitored by pH strips and remained constant at pH $\cong$ 5.5 over the concentration range we discuss in the following. Fig. 4.1a shows an optical image of the FET, which has been used with dimensions: 10 μm × 16 μm × 60 nm (length × width × height).

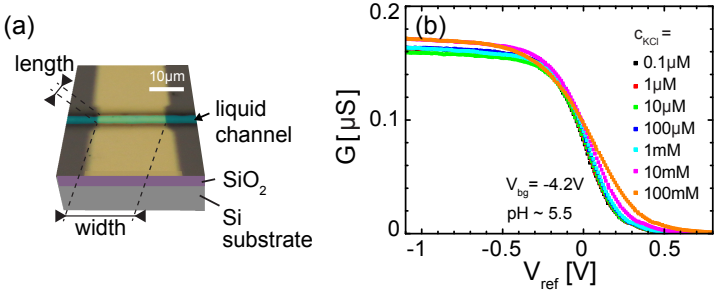


Figure 4.1: **(a)** Optical image of the used ISFET. The ISFET is 10 μm long and 16 μm wide with a thickness of 60 nm. **(b)** Effect of different KCl concentrations dissolved in de-ionized water (constant pH value) on the transfer characteristics as a function of measured liquid potential V_{ref} and at a fixed back-gate voltage V_{bg} of $-4.2\,V$. No shift is observed for concentration up to ∼1 mM. A change in slope of the transfer characteristics for concentrations $\geq 10\,mM$ is visible.

In Fig. 4.1b the electrical conductance G is plotted against V_{ref} at different KCl concentrations and fixed V_{bg}= -4.2 V. In contrast to previous pH measurements, no shift is visible for concentrations <10 mM. The curves lie almost on top of each other. However for concentrations >10 mM a change in slope is visible. To further analyse our observations we measured transfer characteristics for divalent ions as well at different concentrations dissolved in DI water. Again, the pH of the solution was kept constant at pH $\cong$ 5.5. Fig. 4.2 shows transfer curves for $MgCl_2$ and Na_2SO_4 on the linear (Fig. 4.2a and (c) and semi-logarithmic scale (Figs. 4.2b and 4.2d). For concentrations up to 10 mM we observe the same behaviour as for monovalent ions (Fig. 4.1b). The transfer characteristics are not influenced by the ion concentrations in the electrolytic solution over several orders of magnitude. In the linear scale as well as in the logarithmic scale the conductance curves lie almost on top of each other. If the ion concentration is larger than ∼10 mM, most notably a change in slope is observed. This effect is even more pronounced when plotting our findings on semi-logarithmic scale whereas the

subthreshold regime is enhanced. We observe a large shift of $\sim 260\,\mathrm{mV}$ between 10-100 mM (indicated by the horizontal arrow) towards less negative gate voltages independent of the ion valence. The subthreshold slopes deep in the subthreshold regime of the non-shifted as well as the shifted curves remain the same (indicated by dashed lines in Figs. 4.2b and 4.2d).

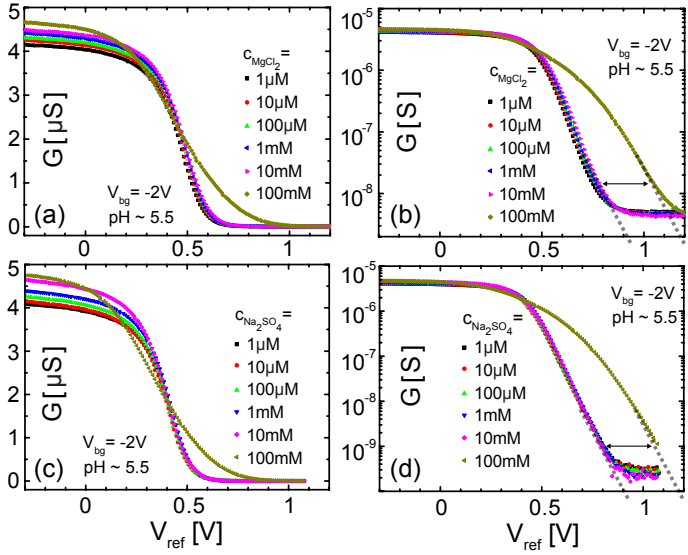


Figure 4.2: Effect on the transfer characteristics for different mono- and divalent ion concentrations dissolved in deionized water at constant pH $\cong$ 5.5 measured as a function of V_{ref} and a fixed V_{bg} of $-2\,\mathrm{V}$. **(a)** Conductance curve changes for different $MgCl_2$ concentrations plotted in linear and semi-logarithmic scale **(b)**. An abrupt change of the transfer characteristics is visible for a concentration $> 10\,mM$. In the logarithmic scale this abrupt change is visible as a transfer characteristics shift. The same effect is observed for different Na_2SO_4 concentrations in linear **(c)** and semi-logarithmic scale **(d)**. The dashed lines in (b) and (d) indicate the slope of the shifted curve with respect to the non-shifted curves. The shift for both salts is $\sim 260\,mV$ (indicated by the horizontal arrows).

4.1.1 Explanation: Ion concentrations <10 mM

Since no shifts are observed for ion concentrations <10 mM, we conclude that the surface potential ψ_0 does not depend on the ion concentration of the salts KCl, $MgCl_2$ and Na_2SO_4. According to the Bergveld model [6] the threshold shift can be described as

$$\Delta V_{th} = -2.3\frac{k_B T}{e} \cdot \alpha \cdot \Delta pH, \tag{4.1}$$

with k_B the Boltzmann constant, T the absolute temperature and e the elementary charge. α is the dimensionless sensitivity parameter, introduced previously (page 41) and is given by

$$\alpha = (C_{dl}/C_s + 1)^{-1} \tag{4.2}$$

where C_s denotes the surface buffer capacitance determined by the density of active surface species and C_{dl} the double-layer capacitance. In the derivation of this formula [6], C_{dl} has implicitly been assumed to be much larger than C_{ox}, C_{NW} and C_{bg} and therefore α may vary between 0 and 1. According to equation (4.1), the highest sensitivity to a pH change is given by $2.3(k_B T/e)$ which amounts to 59.5 mV/pH at room temperature. When using alumina as the interface layer between the FET and the liquid, a pH sensitivity close to the Nernst limit is observed. This shows that $\alpha \cong 1$ and consequently that $C_s \gg C_{dl}$. Equation (4.2) in principle allows a dependence on the ion concentration for a fixed pH value, because the ion concentration c_{ion} enters the double-layer capacitance C_{dl}. However, since $C_s \gg C_{dl}$, α is only weakly dependent on c_{ion}. The ion-induced change in the double-layer capacitance is therefore not visible in ψ_0 and cannot induce a threshold shift. This simple picture may also explain the observed ion concentration dependent shifts measured for the SiO_2 surface [75, 47]. The buffer capacitance of this surface is known to be lower. Instead of the maximum possible threshold shift, one observes in devices with SiO_2 surfaces a shift that is typically reduced by a factor of ≈ 2, see for example Gao et al.[60], while for the Al_2O_3 surface large values approaching the Nernst limit were found in this thesis and have been reported recently [77]. The reduced sensitivity for FETs with SiO_2 surfaces points to a case where $C_s \sim C_{dl}$, yielding an appreciable dependence on the ion concentration c through C_{dl}. The size of this effect will also depend on the actual pH value relative to the point of zero charge (isoelectric point). The presented model is quite tempting as it captures the observation in a qualitatively correct way. However, further work is needed to prove the dependence quantitatively.

4.1.2 Ion concentrations larger than 10 mM

To clarify our observation at concentration >10 mM we first have to distinguish this effect between protons and other types of ions in the electrolyte. For that reason a control experiment was realized where the transfer characteristic of the FET in pH 7 buffer solution and a ten times dilution thereof was measured (Fig. 4.3). The total ion concentration in the buffer solution is $c_{tot} \sim 100$ mM. This concentration is rarefied by factor ten ($c_{tot} \sim 10$ mM) after dilution in DI water. The pH value, as measured by a pH meter and pH strips, remained constant. The most pronounced effect is the slope change (Fig. 4.3). In the logarithmic scale (inset of Fig. 4.3) a shift of ~ 100 mV towards a more negative gate voltage is visible, indicated by the dashed lines.

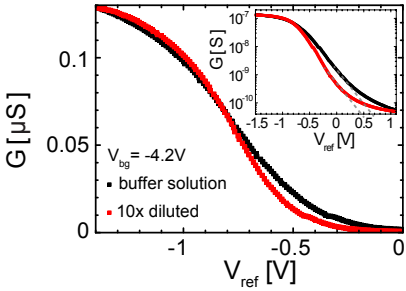


Figure 4.3: Effect of undiluted and ten times diluted pH 7 buffer solution. A slope change is also visible. Inset shows the same data in semi-logarithmic scale. Dashed lines indicate the threshold voltage shift.

To explain the unexpected results we have to analyse the linear regime and the subthreshold regime separately. We start with the subthreshold regime. In this region, the current scales exponentially with gate voltage (equation (1.5), page 5). The slope which can be deduced deep in this regime, the subthreshold swing S is proportional to the gate and FET capacitance

$$S = \ln(10)\frac{k_B T}{q}\left(\frac{C_g + C_{FET}}{C_g}\right).$$

C_g and C_{FET} are the gate oxide capacitance and the nanowire FET's depletion capacitance. Deep in the subthreshold regime were the FET is driven into almost full depletion, $C_{FET} \ll C_g$ and S will be a constant indicated by the dashed lines in Figs. 4.3b and 4.3d. Hence, the observed shift is due

to an additional gating. But where does this sudden gating comes from and why does it happen only at concentrations >10 mM?
In the subthreshold regime only the capacitances play an important role. As we learned in the previous chapter for an open-gate FET in electrolytic solution, the gate oxide capacitance is a series connection of the double-layer capacitance C_{dl} and the TOX capacitance C_{ox} and C_{FET} in the subthreshold regime. For a series connection of capacitances ($\frac{1}{C_{tot}} = \sum_i \frac{1}{C_i}$) the smallest value should dominate. The question which one is dominant is not easy to answer. While C_{ox} remains constant ($C_{tox} \sim 6 \cdot 10^{-13}$ F for the given FET geometry), there are the two other capacitances which have to be analysed. In general, one would expect the nanowire depletion capacitance to be the smallest contributor ($C_{FET} \sim 3 \cdot 10^{-13}$ F with a nanowire thickness of $t_{FET} \sim 60\,nm$), since the double layer capacitance for an electrolyte with a 100 mM ion concentration ($\lambda_D \sim 1\,nm$) is in the range of $C_{dl} \sim 1 \cdot 10^{-10}$ F. However, to this date it is not exactly known how the double-layer with its corresponding C_{dl} influences the electrical properties of a sensor based on a FET [78, 79]. Especially adsorption of (counter)ions in the direct vicinity of the surface, the Stern layer (Fig. 4.4), remains an unknown quantity with many theories and uncertainties [34, 80, 81, 82].
We suggest that the mechanism for the observed shift is due to forced accumulation of charges at the FET surface by the applied liquid potential. As we explained in the previous section, a double-layer with its typical screening length (equation (2.2), page 20) is formed in the vicinity of the surface. This double-layer is a complex region. Counterions approach interfacial charges to screen them, in our case protonated or deprotonated hydroxyl groups (Fig. 4.4a). Ions in an electrolytic solution have a spatial distance, d_{ion}, between each other. Depending on the concentration and the type of ion d_{ion} can be calculated, e.g., for 100 mM KCl $\rightarrow d_{ion} \sim 2.5$ nm, for 10 mM KCl $\rightarrow d_{ion} \sim 5.5$ nm, for 1 mM KCl $\rightarrow d_{ion} \sim 12$ nm.

An external applied liquid potential will force the accumulation of a significant amount of additional charges at the FET's surface [83]. The Stern layer will become more densely packed with d_{ion} decreasing until it reaches a minimum defined by the ionic radius (typical values 0.3- 2 $\AA$). A denser packing is not possible due to electrostatic interactions between the ions. However, if this is the case, the double-layer will collapse at a certain point and the charge neutrality will be lost. A complete shielding of the accumulated charges is not possible (Fig. 4.4b). In a capacitor picture, the second plate will be moved to infinity, hence $C_{dl} \rightarrow 0$, and thus C_{dl} becomes the dominant capacitance in our series connection. The potential of these non-screened charges will have an effect on the conductive channel in the FET acting as an additional gate. Since we observe a transfer-curve shift to the right, the additional charges must be negative. Taking into account the ob-

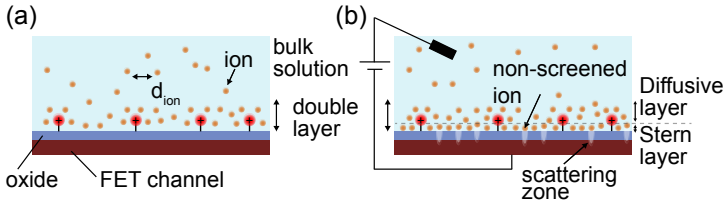


Figure 4.4: **(a)** The protonated hydroxyl groups at the FET surface are screened by ions in the solution forming a double-layer. Ions in the electrolyte have a typical distance d_{ion} between each other. **(b)** If a liquid potential is applied a significant amount of additional ions are forced toward the surface (Stern layer) and d_{ion} decreases. Some ions remain unscreened causing a gating in the FET channel.

served shift of $\Delta V \sim 0.3\,V$, we can estimate a lower limit of the number of charges, N, needed to induce such a shift using $N = C_{dl}U/q$. Depending on the value of C_{dl} we can estimate $N \hat{=} 10^8 - 10^9$ which can be related to 0.6-6 ions/nm^2. For such an amount of charges in the direct vicinity of the surface the average distance between ions corresponds to $d_{ion} \sim$ 0.4-1.3 nm. This number is certainly smaller than the distance one would expect for an ion concentration of 100 mM. For the case where $C_{dl} \to 0$, one could also imagine a denser packaging of ions. The non-screened ions may influence the charge carrier in the channel and thus we have to analyse the linear regime as well.

As we introduced on page 3 the source-drain current of a FET in the linear regime is well described by

$$I_{sd} = \mu \frac{W}{L} C_g V_{sd} V_g.$$

The slope of the tangent at the inflection point of the transfer curve results in the transconductance $g_m = \frac{I_{sd}}{V_g} = \mu \frac{W}{L} C_g V_{sd}$. While V_{sd} and the FET geometry remain unchanged, $g_m \propto \mu C_{lg}$. Here, C_{lg} is the series connection of C_{dl} and C_{ox} (page 40). Fig. 4.5a shows the extracted transconductance values (e.g., linear fits in Fig. 4.2a) plotted against the ion concentration for various salts dissolved in DI water. For a concentration of 100 mM the transconductance decreases since the slope of the transfer characteristics is also reduced. In Fig. 4.5b we plot the transconductance for a thinner ISFET (width $\sim 2\,\mu$m). We observe a similar tendency albeit not changing

as abrupt as observed for the larger FET. Using our previous argumentation ($C_{dl} \rightarrow 0$) for increasing c_{ion}, g_m will decrease since $C_{lg} \rightarrow 0$. This may explain the transconductance decrease.

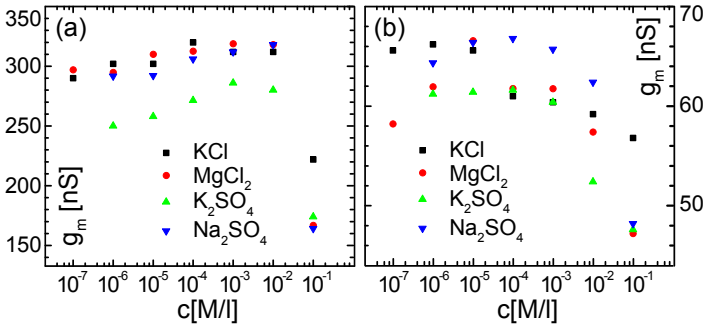


Figure 4.5: **(a)** Extracted transconductance g_m values for various salt concentrations and salts for the FET shown in Fig. 4.1a with a width of $\sim 16\,\mu m$ and in **(b)** for an FET with a width of $\sim 2\,\mu m$. For large concentrations the transconductance decreases.

However we have to keep in mind that g_m may also be influenced by a changing mobility since $g_m \propto \mu C_{lg}$. If additional charges are forced to approach the FET surface while not being screened, their potential may interfere with mobile charge carriers in the FET channel (Fig. 4.4b). In a simple picture these charges can act as scattering centres which will cause a mobility change visible as a slope change in the linear regime of the transfer characteristic. As more and more charges accumulate this slope change will be more pronounced. On the other hand if the bulk electrolytic solution contains less ions (smaller concentrations) a higher liquid potential has to be applied to reach the critical density to act as an additional gate. This may explain why the slope change is only observed for concentrations >10 mM. To prove our model we are currently investigating additional supporting experiments to analyse our findings.

Alternative explanation

In the previous chapter we argued that a maximum possible threshold voltage shift can only be expected if the surface pH, pH_S^+, remains constant (page 33) and the oxide has a high buffer capacity ($\alpha \sim 1$, page 41). Only for this combination

$$\Delta V_{th} = -2.3\frac{k_B T}{e} \cdot \alpha \cdot \Delta\text{pH} = -2.3\frac{k_B T}{e} \cdot \alpha \cdot (\Delta pH_S^+ - \Delta pH_B^+) \qquad (4.3)$$

will result in the maximum Nernst limit response of $\sim 60\text{mV/pH}$ at room temperature. In aqueous solutions, the (-OH) groups of an oxide remain undissociated as long as the pH value of the liquid is the same as the isoelectric point (IEP). For the case of Al_2O_3, IEP is at pH $\sim$ 9 [65]. Since Al_2O_3 has an $\alpha \sim 1$, pH_S^+ remains constant at pH $\sim$ 9, even if the pH value of the bulk solution, pH_B^+, is changed. In the absence or at low background ion concentration the equilibrium dissociation constants for the possible reaction of the protons, H^+, and the (-OH) groups can be calculated

$$K_a = \frac{\nu_{MO^-} a_{H^+}}{\nu_{MOH}} \quad and \quad K_b = \frac{\nu_{MOH} a_{H^+}}{\nu_{MOH_2^+}}.$$

A more detailed discussion can be found in appendix C on page 110. However, if the background ion concentration is high enough and not negligible, it might be possible that the reactions start to drift away from equilibrium. The background ions interfere with the proton/OH-group reactions. At a certain concentration the surface will not be able to buffer proton concentration changes at its direct vicinity and pH_S^+ will adjust itself to become equal to pH_B^+. In our case the surface pH of $\sim$ 9 will change to adapt the solution's pH of $\sim$ 5.5. By doing so the nanowire sensor will response by a threshold voltage shift. This shift can be calculated to be of the order of $\sim 240\,\text{mV}$ using the high pH sensitivity of alumina, which is close to the Nernst limit and a ΔpH_S^+ of 4. This value is comparable with the shift of $\sim 260\,\text{mV}$ we observe in our experiment (Fig. 4.2). For the case of the diluted pH buffer (Fig. 4.3) we observe a shift of $\sim 100\,\text{mV}$, which is also in agreement with a calculated threshold shift of $\sim 120\,\text{mV}$. Here, pH_S^+ shifted by two values to pH 7. The alternative explanation does not cover the slope change which we observed in the linear regime. To validate this theory more experiments are currently investigated to prove its correctness.

4.2 Summary

In summary, we demonstrated that using an Al_2O_3 interface between the FET's surface and the liquid results in an insensitivity to monovalent as well as divalent ions at a large concentration range up to 10 mM. This makes the Al-oxide an interface of choice for pH sensing applications as this interface guarantees a high pH sensitivity independent of the background ion concentration, an important factor in e.g. biological experiments. When it comes to sensing of small ions other than protons, FETs with an Al-oxide surface can be used as reference electrodes. In order to be selective to ions, the surface needs be functionalized, e.g., by crown-ethers or silanes [84]. Such a functionalization will allow us to combine the physical properties of our sensor with chemical specificity. We will discuss this topic in the next chapter. We could already show that even a system with only a simple salt dissolved in deionized water results in unexpected FET responses. This observation shows that there is much more to explore in the vicinity of the FET surface surrounded by an electrolyte. Above a concentration of 10 mM we observe a sudden transition resulting in a transfer characteristics change. This highly interesting effect may be due to forced accumulation of charges at the FET surface or due to an adjustment of the surface pH to the bulk pH. The experiments give first hints and the presented evaluation and the models have to be considered as work in progress. The threshold voltage analysis we have presented so far may be distorted by the slope change of the transfer curves. To overcome this issue observed shifts should be analysed in the subthreshold regime.

5 Additional Investigations

So far we have studied the sensing capabilities of our fabricated nanowire FETs. In this chapter we will describe additional experiments which were conducted during this thesis and will be of importance for future studies. We will briefly discuss the signal-to-noise ratio in our fabricated nanowire FETs. Then we will focus on surface functionalization and passivation studies which were conducted. As a last step, we will describe the up-scaling of our measurement setup and introduce the nanowire FET pixel structure, which was developed for future (bio-)chemical studies.

5.1 The detection limit of nanowire FET sensors

The strive for nano-scale FET devices with the focus on (bio-)chemical sensing has lead to the fundamental question of the detection limit achievable with nano-scale devices [85]. In order to reach the detection limit, intense attempts have recently been made to understand the factors determining the signal-to-noise ratio (SNR) [60, 67, 86, 87]. While it has been claimed that the SNR increases in the subthreshold regime, a more detailed understanding of the noise properties is needed to optimize the SNR across the full operating range of the FET.

To determine the sensing limit of our nanowires, we have conducted experiments on the noise properties sensor (Fig. 5.1a). This topic will be covered

in detail in the PhD thesis of Alexey Tarasov [88], while we will give here an overview and discuss this topic in short.

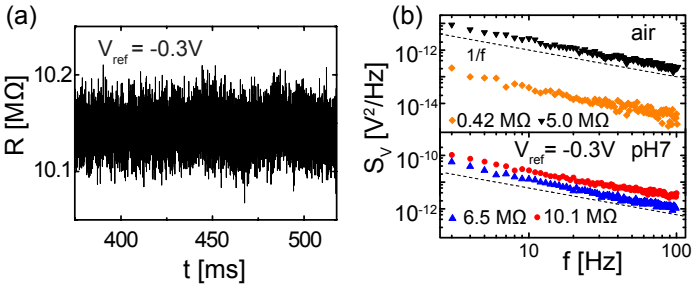


Figure 5.1: **(a)** Typical resistance fluctuation versus time at a fixed working point (liquid potential of $V_{ref} = -0.3V$). The noise is obtained from the temporal dependence of the source-drain current I_{sd} using fast Fourier transform. **(b)** Noise power spectral density of the voltage fluctuations S_V obtained for a source-drain bias voltage of $V_{sd} = 90\,\mathrm{mV}$ for different resistances of a nanowire measured in air and in a pH 7 buffer solution. The dashed lines indicate a $1/f$ slope.

Fig. 5.1b shows the frequency dependence of the voltage noise power $S_V(f)$ of the wire for different resistance values, measured in air and in a pH 7 buffer solution at a fixed liquid-gate voltage of $V_{ref} = -0.3V$. The source-drain current I_{sd} through the nanowire was measured by a current-voltage converter with a variable gain ($10^5 - 10^9\,\mathrm{V/A}$, $V_{sd} = 10 - 100\,\mathrm{mV}$). The voltage noise power spectral density S_V was determined through a fast Fourier transform of the time dependent fluctuations of I_{sd}. Since the low frequency noise is determined by resistance fluctuations it is therefore of 1/f type. Such a behaviour can be described phenomenologically by Hooge's law [89, 90]

$$S_V(f) = V_{sd}^2 \frac{\Gamma}{Nf}. \tag{5.1}$$

The material dependent parameter Γ accounts for scattering effects, and the constant N denotes the number of fluctuators in the system.

To relate the measured noise to our sensing experiments we define the noise power of the threshold voltage δV_{th}, since the physical signal in FET sensors is the threshold voltage shift (chapter 3). δV_{th} is given by

$$\delta V_{th} = \frac{\sqrt{S_V/V_{sd}^2(f)}}{g/G} = \frac{\sqrt{S_V/V_{sd}^2(f)}}{(\ln G)'}. \tag{5.2}$$

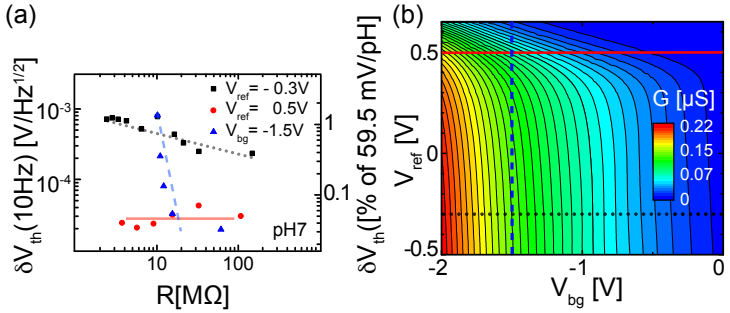


Figure 5.2: **(a)** Threshold voltage fluctuations $\delta V_{th}{=}S_V/(\ln G(V_{ref}))'$ in pH 7 buffer solution as a function of the resistance R. Data points were calculated from extracted noise values from (b) at 10 Hz. Solid, dashed and dotted lines are guides to the eye. The right axis shows δV_{th} relative to the Nernst limit of the pH sensitivity (59.5 mV/pH at 300 K). **(b)** 2D-conductance map $G(V_{bg}, V_{ref})$ of a nanowire FET in pH 7. Noise measurements were conducted along the solid, dashed and dotted lines.

In Fig. 5.2a, δV_{th} is plotted for the measurements along the lines in Fig. 5.2b. We observe that in the nanowire-dominated regime (●) δV_{th} is almost two orders of magnitude smaller than in the contact-dominated regime (■). The data obtained at a fixed V_{bg} and varying V_{ref} (▲) demonstrate the cross-over between the two different regimes. This shows that the gate-coupling to the liquid is a crucial factor determining the ultimate sensitivity. We can confirm recent studies on the on subthreshold SNR [60]. However, δV_{th} can be low over an extended range of nanowire resistance values R, from $\sim$ 1 to 100 MΩ. This range covers the transition from the linear to the subthreshold regime. The resolution limit of these SiNW-FETs corresponding to less than 0.1% of of a typical Nernstian pH shift in one Hz bandwidth (Fig.5.2a, right axis) throughout the full resistance range.

5.2 Surface functionalization and passivation

Throughout this thesis we investigated reproducibility, stability and sensing capability of our fabricated nanowire field-effect transistors. As long as an oxide surface builds the interface between the open-gate FET and the electrolytic solution it will remain sensitive only to pH changes (chapter 4). Hence, any pH change of the bulk solution or in direct vicinity of the surface will be sensed by the nanowire FET. To target specificity of analytes in solution the surface has to be (i) passivated against pH reactions and (ii) functionalized for specific targeting [84, 91]. To address this issues we investigated passivation and to functionalization of the surface. As a starting point we chose amino-propyl-thriethoxy-silane (APTES), sketched in Fig. 5.3a. It is well suited to bind covalently to (-OH) groups at the oxide surface and forms, in the ideal case, a monolayer, covering the whole surface. Further, it has a reactive amino group (NH_2^+), which can be used for further bounding of molecules as sketched in Fig. 5.3b [92].

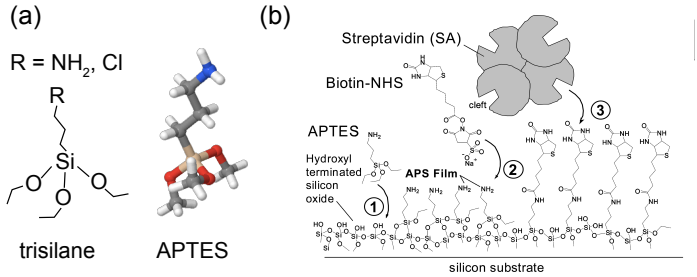


Figure 5.3: **(a)** Typical structure of a trisilane and its 3D structure. R denotes the end-group of the molecule, e.g. NH_2 for amino-propyl-thriethoxy-silane (APTES) and Cl for chloro-propyl-thriethoxy-silane (CPTMO). **(b)** Necessary steps to attach biomolecules to a silicon oxide surfaces: the APTES molecules are covalently bound to silicon oxide forming a 3-aminopropylsiloxane (APS) film with Si-O-Si bonds to the surface (1). Biotin-NHS is covalently bound to the amine-terminated surface forming amide bonds (2). Then streptavidin (SA) is biospecifically attached to biotin via the SA cleft (3). Adapted from [92].

To form the monolayer, APTES has been vapour-deposited on the nanowire FET and subsequently been annealed to crosslink the silane (appendix B). For a better comparison of results with and without functionalized surfaces, the same nanowire FET that has been used in chapter 3 was chosen. The APTES-functionalized sensors were then exposed to pH buffer solutions and the pH sensitivities were extracted.

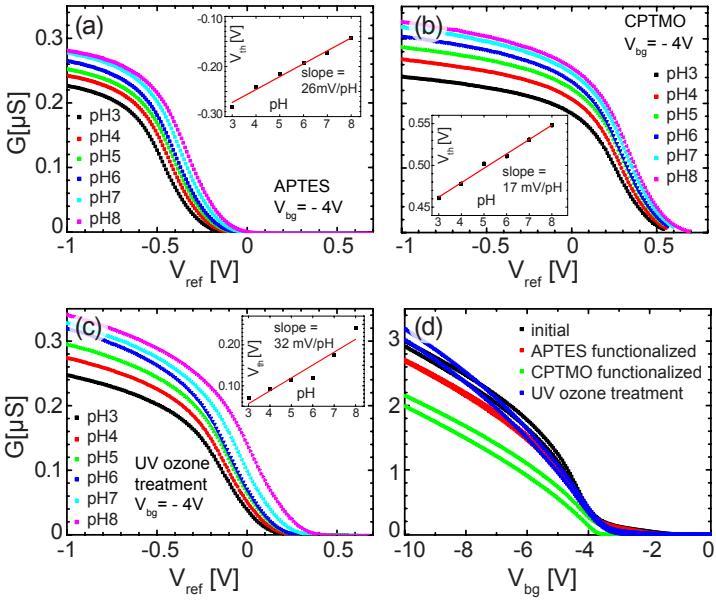


Figure 5.4: Effect of pH change on the transfer characteristics measured as a function of V_{ref} and V_{bg} after covering the device surface with different silanes. In **(a)** the effect is shown by the set of $G(V_{ref})$ curves for a fixed V_{bg} of -4 V and different pH values with an APTES covered surface, whereas in **(b)** the surface was additionally covered with CPTMO. For both cases a decrease in sensitivity is observed (insets). After a UV ozone treatment the sensitivity increased again **(c)**. For comparison the electrical conductance G is shown as a function of back-gate voltage V_{bg} measured in ambient after the various surface treatments shown in (a)-(c).

Fig. 5.4a shows the transfer characteristics for different pH buffer solutions at a fixed back-gate voltage of -4 V. The inset of the graph shows the extracted sensitivity (ΔV_{th} versus pH value). Compared with a bare alumina surface exposed to pH buffer solutions (chapter 3, Fig. 3.5), we observe a sensitivity decrease of factor ~ 2. We derive a value of ~ 26 mV/pH. Even so the device surface is functionalized (passivated) with the APTES monolayer, it still tends to respond to pH changes. In the next step the sample was covered by an additional silane. This time we choose chloro-propyl-thriethoxy-silane (CPTMO) as depicted in Fig. 5.3a. This silane has an non-reactive chloro-group (-Cl) at one end. After vapour-deposition of CPTMO on the device the performance was measured again in different buffer solutions (Fig. 5.4b).

Note that by accident the previous silanization layer has not been removed. Again we observe a decrease in the sensitivity (inset of Fig. 5.4b) by a factor of ~ 1.5 to be $\sim 17\,\mathrm{mV/pH}$.

To explain our observations we have to take a closer look on the oxide surface. As mentioned previously the outer most layer of an oxide consists of hydroxyl groups, in the case of alumina $15\,\mathrm{groups/nm^2}$ [65]. These groups can undergo a reaction with silanes forming covalent bonds [92]. The APTES is a rather bulky three-dimensional molecule (Fig.5.3a). Each leg will, ideally, bind to a hydroxyl group, thus passivating the surface against de- or protonization. The silanized surface has accessible $(-NH_2^+)$ groups in a distance of $\sim 1\,nm$ to the surface [93], which can be used for further attachments of molecules (Fig. 5.3b). However, even so APTES functionalized surfaces are often described as uniform monolayers, it is very unlikely that such dense films exist [94, 95]. A non-uniform layer (or even multilayers) is more likely formed as sketched in Fig. 5.3b. The lack of order will result in layer defects and inaccessible amine groups. The coverage and the accessible amino groups strongly depend on the deposition method. In case of APTES this accessibility can vary between a few $(-NH_2^+)$ groups per $100\,nm^2$ up to a few 100 groups per $100\,nm^2$ [95]. The surface tends to still have a large amount of accessible (-OH) groups, which are still reactive to pH changes (Fig. 5.5).

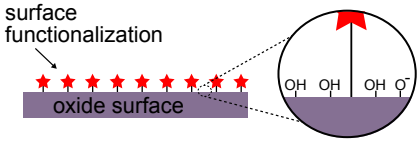


Figure 5.5: Sketch of a functionalized surface with accessible hydroxyl groups (-OH). Not to scale.

In contrast to a non-functionalized surface, the pH sensitivity should be smaller, what we observe. At this point, it is important to realize, that this pH sensitivity, even though small, will interfere with the desired surface reactions and its detection. To further decrease the amount of accessible (-OH) groups, an additional silanization can be performed. In our case CPTMO has been vapour-deposited in a second silanization process. This silane, similar to APTES, bind also covalently to the surface hydroxyl groups. The reactions will additionally decrease the amount of accessible hydroxyl groups. As result, we observe a further decrease in the pH sensitivity. Now one could ask whether this effect is reversible and if it is possible to recover the

original sensitivity of ∼50 mV/pH by stripping away the silanes. To answer this question we exposed the device to UV ozone for several minutes. UV ozone is known to react with organic compounds and as a result silanes on the surface should be removed [96]. After this treatment the pH response was measured again. Fig. 5.4c shows the transfer characteristics for different pH values with their corresponding pH sensitivity (inset of Fig. 5.4c). We observe a sensitivity increase by almost a factor 2 to be $\sim 32\,\mathrm{mV/pH}$. This value is slightly smaller compared to the previously extracted value of $\sim 50\,\mathrm{mV/pH}$ (chapter 3). This lower value may be attributed to silane residuals on the surface. Fig. 5.4d shows the transfer characteristic in ambient plotted as a function of the applied back-gate voltage after the different treatments. After the UV ozone treatment the initial characteristic is almost restored. Our observations give a first hint. More experiments have to be addressed to fully understand the effects.

5.2.1 Summary

We have shown that the pH response of a nanowire FET can be decreased by a functionalization/passivation process using different silanes. The remaining small sensitivity can be attributed to non-passivated hydroxyl groups which are still able to undergo a reaction with protons in the electrolytic solution. In contrast to multi-leg silanes, simple-leg silanes should be much better in forming monolayers (appendix Fig. A.4, page 84). It is of great importance to fully control the surface of the sensor. Otherwise it will not be possible to differentiate between signals coming from pH reactions at the surface and the desired chemical reaction of a target molecule. In contrast one could use the high pH sensitivity in the direct vicinity of the surface. It is well-known that many bio-chemical reactions locally change pH values [97], an effect which can be exploited for indirect measurements.

5.3 Thinking big: nanowire FET array sensors

Up to now we have demonstrated reproducible experimental results with single silicon nanowire field-effect transistors. However, for practical applications, like wearable and portable sensor devices it is important to do multiplexing, e.g., differential measurements to combine information [56]. For that reason a new measurement platform has been built allowing to go beyond individual measurements. This platform comprises a new automated measurement setup as well as a new chip design consisting of 48 individually addressable nanowire FETs.

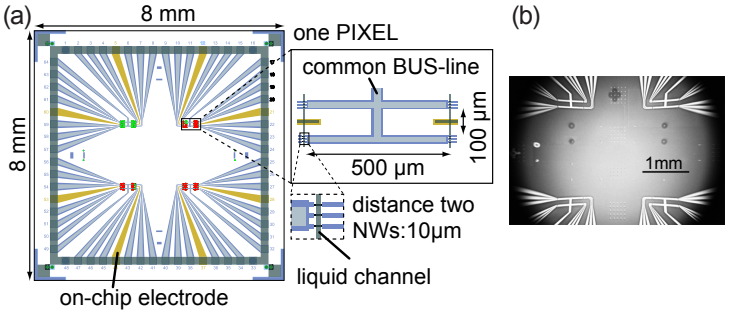


Figure 5.6: (a) Schematics showing the new 'pixel' structure with 48 individually-addressable nanowire FETs. 4 groups of 3 nanowires are grouped together in a pixel. 4 pixels are integrated on one chip with liquid channels (gray). Each channel can be addressed with on-chip gate electrodes (yellow) for local liquid gating. **(b)** SEM picture of a fabricated pixel structure. Picture by courtesy of K. Bedner.

Fig. 5.6a shows the new designed chip. Here, 4 groups of each 3 silicon nanowires are grouped together for redundancy in what we term a 'pixel'. The 12 wires are connected via a common bus-line while being individually-addressable. In total, 4 pixels are integrated together with 8 on-chip electrodes for local liquid gating (yellow in Fig. 5.6a) and one common back-gate. The design enables new experiments, e.g., time-resolved correlation measurements as well as differential measurements using multiple functionalization, which is beyond the scope of this thesis. The new design has been realized by means of UV lithography. A recently initiated additional research consortium (NanowireSensor) within the Nano-Tera[1] project allows the fabrication of pixel devices using a state-of-the-art e-beam writer and is realized together with the PSI located in Villigen, Switzerland. Furthermore the cooperation

[1] Nano-Tera is a Swiss federal program funding research projects.

allows other investigations and experiments, e.g., contact doping (chapter 2, page 26), width dependence and similar. Fig. 5.6b shows an SEM image of an e-beam fabricated pixel-structure.

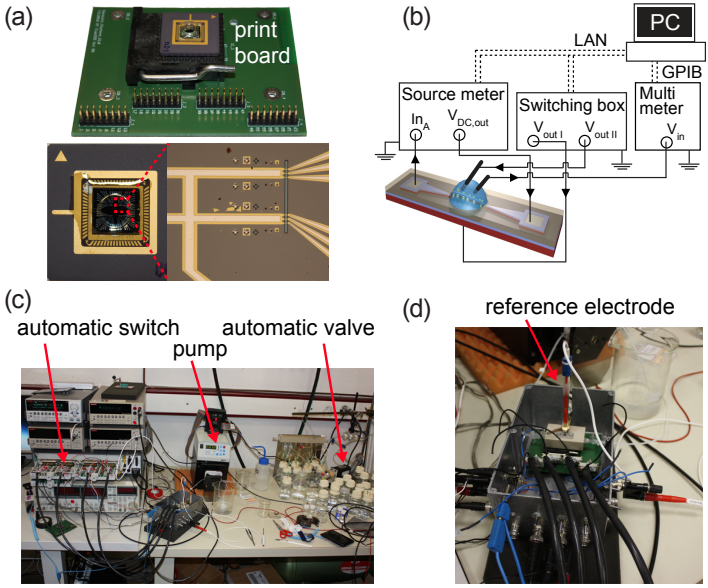


Figure 5.7: **(a)** Optical image of the print board containing a zero-insertion-force socket and a fabricated chip fixed on a chip carrier with the liquid channel running vertically. **(b)** Schematics of the upscaled measurement setup. **(c)** Optical image of the new setup which includes an automatic switch for multiplexing, a PC-controlled pump as well as an automatic valve. **(d)** Optical image of the system in use.

To address electrical measurements and multiplexing using the new structure, the measurement setup had to be enlarged. A home-designed and built print board with a zero-insertion-force socket allows the direct connection of pixel devices to an automatic multiplexer unit via a chip carrier (Fig. 5.7a). A schematic of the upscaled measurement setup is shown in Fig. 5.7b. The multiplexer can automatically switch between different nanowire FETs allowing parallel measurements. In addition, an automatic pump and valve are connected to the new setup. Fig. 5.7c shows an optical image of the new setup and the fully equipped system in use (Fig. 5.7d). The system is fully controlled by a PC and a self-written LabView program while being able

to run automatically, switching between different nanowire FETs, pumping and changing solutions.

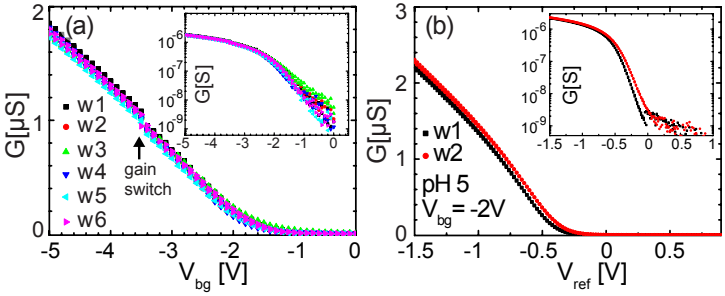


Figure 5.8: **(a)** Conductance G as a function of V_{bg} in forward and backward direction for six different wires under ambient conditions demonstrating the excellent reproducibility with negligible hysteresis. The arrow indicates the gain switch of the measurement electronics. The inset shows the same data on a log scale. **(b)** Conductance G as a function of V_{ref} and $V_{bg} = -2\,V$ in forward and backward direction for two wires in pH 5 buffer solution. Their characteristics lie almost on top of each other with a non measurable hysteresis ($H_{th} \sim 0\,mV$), even in liquid environments. The inset shows the same data in a log scale. Data obtained from two different samples.

As mentioned previously reliable and reproducible sensors are crucial for sensing experiments, since this relies on the accurate measurement of the threshold voltage shifts. We have measured in parallel the transfer characteristics of different nanowire FETs on a single pixel structure. In Fig. 5.8a the transfer characteristics for six different SiNW FETs out of the twelve is shown on a linear and logarithmic (inset) scale while sweeping the gate-voltage forth and back. Although the shown device is one of the first chips produced with the new structure, the curves align almost perfectly on top of each other while showing a non-measurable hysteresis ($H_{th} \rightarrow 0\,\mathrm{mV}$). In addition to characterization in ambient, different nanowire FETs on the pixel structure have been measured in electrolytic environments. Fig. 5.8a shows the transfer characteristics of two different nanowire FETs as a function of V_{ref} and $V_{bg} = -2\,V$ in pH 5 buffer solution in forward and backward direction. Here again, the nanowire FETs align almost on top of each other while showing a non measurable hysteresis ($H_{th} \rightarrow 0\,\mathrm{mV}$). With the new pixel structure and the multiplexing setup, we have set the foundation for further experiments with ions and biomolecules. A new set of measurements is within reach to explore the use of nanowire FETs for future applications as chemical and biochemical sensors.

5.4 Towards specific (bio-) chemical sensing with nanowire FETs

At this point of the thesis it is time to recline and to look back. We demonstrated reproducibility with single nanowire FETs as well as with nanowire FET arrays. We investigated their sensing capabilities, showed pH sensitivity and explored their sensing ability to different kinds of ions. We studied the detection limit, surface functionalization and passivation schemes. At this juncture the sensing platform is ready to target the next step: specific (bio-) chemical sensing. In order to work towards this goal we have to merge all the knowledge we gained. Specificity and versatility imply a surface functionalization in such a way, that measured signals will become reliable, reproducible and trustable. Here we have to distinguish between chemical sensing, e.g., the detection of heavy metal ions, and biochemical sensing, where one aims at detection of specific binding reactions biomolecules with corresponding receptors. Both paths can be realized with our nanowire FET platform.

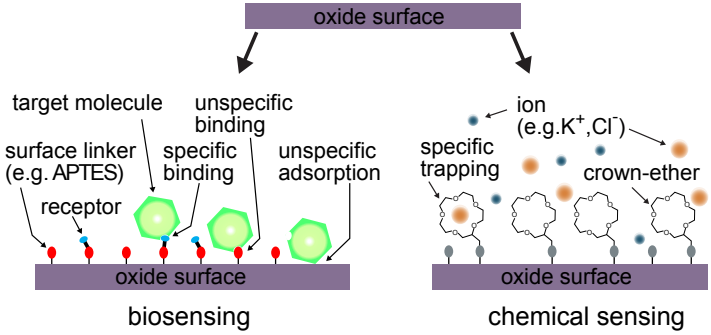


Figure 5.9: Different oxide functionalization schemes toward (bio-) chemical sensing (not to scale). To target specificity the FET's surface needs to be functionalized. Starting from an oxide surface necessary steps are a linker group functionalization followed by attachment of the specific binding agent. In the sketched case this can be either a specific receptor (biosensing) to bind molecules or proteins or a crown-ether attachment as it can be used for specific ion trapping (chemical sensing).

In Fig. 5.9 two different functionalization schemes for chemical as well as biochemical sensing are sketched. Starting from an oxide surface, like SiO_2 or Al_2O_3, a specific functionalization scheme will allow to target specific sensing. The main problem lies within excluding signals resulting from unde-

sired processes, e.g., unspecific binding or adsorption as previously learned.

To go beyond simple ion detection, we recently initiated within our research consortium the detection of different lectins, which are important for a large number of biological processes [98]. Lectins are sugar-binding proteins and are highly specific (affine) to certain sugar moieties. Optimizing ligand binding and the affinities are crucial for designing and finding new powerful drugs, e.g., against diabetes. Hence it is of importance to find proper ligands. The developed platform may help in working towards this direction. It is however important to realize that given the complexity of the surface and its functionalization, each step in functionalization has to be understood properly. In the prospective in understanding our system we started to investigate adsorption of the well known biotin-streptavidin system with different functionalized nanowire FET surfaces[2] to become acquainted with biological agents.
Streptavidin (SA) is known for its very high affinity to biotin with an association constant $K_a \sim 10^{15} M^{-1}$ [92, 99]. This large binding affinity makes the system interesting to grasp knowledge on the detection of the protein-ligand binding reactions. In addition, this system is stable under different conditions, e.g. extreme pH and temperature. The attachment of biotin to an oxide surface is sketched in Fig. 5.3b. As first step the surface is functionalized with APTES forming a film. Then biotin 3-sulfo-N-hydroxysuccinimide (biotin-NHS) is covalently bound to the amino-terminated surface. Now SA can specifically attach and bind, a reaction which should be detectable with our assay system. However, since many functionalization steps are necessary prior to a biotin-streptavidin reaction there might be unintended signals arising from non-specific binding or non-specific adsorption (Fig. 5.9) on the surface. To exclude wrong conclusions it is therefore important to analyse the nanowire FET after every functionalization step. To understand our system we started with the analysis of non-specific adsorption.

Fig. 5.10a shows a first preliminary result of the conductance time-response of the electrical conductance of two APTES functionalized nanowire FETs (pixel structure device) while alternating between phosphate buffered saline (PBS) solution and different concentrations of streptavidin solutions (0.5-5 μg/ml in PBS). Both nanowire FETs show a similar response while introducing the different solutions. In addition to the conductance increase and decrease while introducing the solutions, we observe an overall background conductance decrease over time ($\sim$10 nS after 900 s). This drift may be due

[2]Surface functionalizations in collaboration with J. Kurz, and U. Pieles, FHNW, Switzerland.

to the surface equilibration with the surrounding liquid. However to fully understand this drift more experiments have to be addressed. Fig. 5.10b shows the measured liquid potential V_{ref} while alternating between solutions. V_{ref} fluctuates ∼20 mV over time. These fluctuations correlate with the injection of the different solutions (indicated by the vertical arrows). We can imagine interactions of the SA with the Pt or the reference electrode.

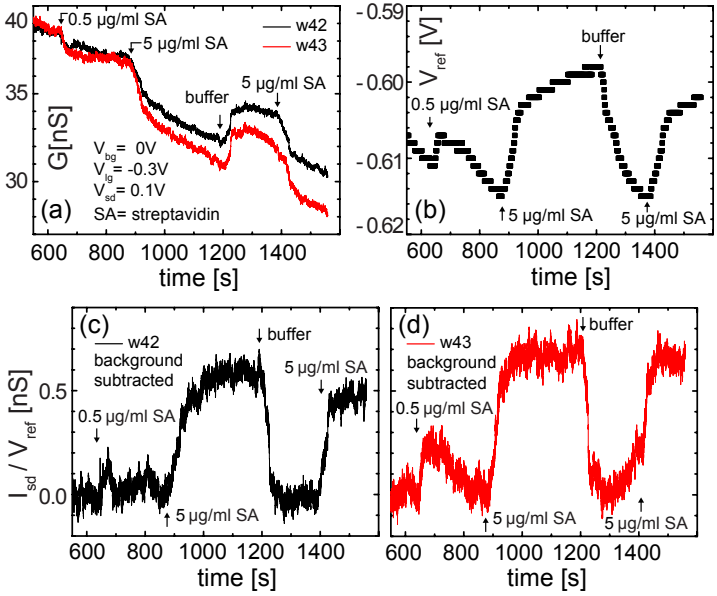


Figure 5.10: **(a)** Preliminary results of non-specific streptavidin (SA) binding on an APTES functionalized nanowire FET surface. The conductance G change over time for two nanowire FETs on one device is shown while changing the solution (buffer: phosphate buffered saline (PBS), SA dissolved in PBS). **(b)** Measured liquid potential over time. **(c)** and **(d)** show I_{sd}/V_{ref} changes versus time for two nanowire FETs shown in (a). The background has been subtracted from the data for clarity. Both sensors show similar behaviour.

For an APTES functionalized surface we expect no SA binding reactions to occur. Any binding or adsorption, which may happen, is non-specific and should be releasable. Figs. 5.10c and 5.10d show the response of the nanowire FETs after background subtraction. As pointed out in Fig. 5.10b the spurious liquid potential fluctuations should be compensate to isolate

the response of the wire and to remove the drift. Hence, measured currents have been divided by V_{ref}. By doing so, the signal change should be only an effect of the wire. After each introduction of SA solutions we observe a conductance increase ($\sim$650 s, 850 s, 1400 s). Both wires respond similarly. For an SA concentration of 0.5 μg/ml in PBS we observe a little increase of conductance which decreases shortly after. However, for a higher concentrated SA solution (5 $\mu g/ml$ in PBS) we observe a clear signal change. The conductance increases by $\sim$700 pA/V for both wires. Since no binding should happen between SA and the APTES the effect can be related to non-specific SA binding with the silanized surface. In other words, if non-specific binding takes place, we should observe the opposite once the SA is released from the surface. After introducing pure PBS we can observe the signal decreasing to its initial value. Non-specific adsorption is responsible for the signal and shows the importance of understanding all steps of functionalization. To further analyse our results and to explain our observations, we are currently investigating more experiments into this direction.

5.4.1 Summary

To summarize this last section we showed a first experimental set towards nanowire FETs as biochemical sensors. Even so the results are not completely understood in full detail, they are promising and motivate for further research towards chemical and biochemical silicon nanowire FET sensors. Further experiments will successfully pave the way to use our nanowire FETs for the detection of more complex protein-ligand reactions or specific chemical sensing. However as we have seen, it is of high importance to fully characterize the nanowire FET sensor to quantify signals and to differentiate between spurious ones.

6

Final Remarks and Outlook

Individual silicon nanowire FETs and nanowire FET arrays follow the direction of signal-based amplification. Their large surface-to-volume ratio makes them highly sensitive down to the molecular level with the ability of high-density integration. An assay built from silicon nanowire transducers can be realized on portable CMOS-compatible chips combining multiplexing capabilities such as simultaneously sensing of pH, of different ion concentrations, small molecules or proteins. In this manner, versatility and selectively can be combined to build a powerful and multifunctional sensing tool.
In this thesis we set the ground for top-down fabricated silicon nanowire field-effect transistors for their future use as chemical and biochemical sensors. We developed a fabrication protocol yielding nanowire FETs with a high degree of reproducibility. This feature is key issue for the reliable performance of sensing devices. For the detection of chemical or biological agents, stable working conditions in electrolytic solutions is mandatory. We could achieve this by eliminating leakage current issues. Introducing the dual-gate approach we could successfully demonstrate the use of these devices as pH sensors. While the dual-gate method allows signal amplification it can also be of great help for increasing the signal-to-noise ratio. The high pH sensitivity can be exploited for indirect measurements of biochemical reactions. Surprisingly even simple ions can lead to unexpected observations, which shows that there is truly more to explore using nano-scaled transducers. On the other hand it clearly demonstrates that controlling and understanding

the transducer-electrolyte interface is an additional key issue to target. The interplay between the (bio-)chemical and the physical world on the nano-scale implies an interplay between chemists, biologists and physicists on the macro-scale to target specificity. For the detection of biochemical binding reactions, the liquid potential has to be monitored. It is therefore of great importance to integrate on-chip reference electrodes within a signal-based amplification assay for differential signal readout; today still an open issue. The developed sensing platform will allow us to conduct further experiments to explore the use of nanowire ion-sensitive field-effect transistors as (bio-) chemical sensors.

To put it succinctly – a completely new window of possibilities has opened up using nano-transducers with their almost infinite capabilities. The signal-amplification path showed its ability to meet today's needs for improving our overall quality of life. These new opportunities are at present [1] "redefining the analytical benchmarks for sensitivity, selectivity and versatility".

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A

Supporting Measurements

A.1 AC-DC bias voltage

In chapter 1 we argued that the transfer characteristics is independent of whether an AC or a DC source-drain voltage (V_{sd}) is applied. Fig. A.1 shows the source-drain current I of a nanowire FET as a function of the back-gate voltage V_{bg} for different AC (317 Hz) and DC source-drain voltages. The curves lies on top of each other.

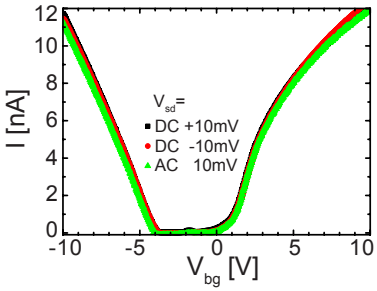

Figure A.1: Current I vs. applied back-gate voltage for different AC (317 Hz) and DC source-drain voltages.

A.2 2d Maps: additional device

The result in chapter 3 has been confirmed with several samples having different top-oxide layer thicknesses. We have shown pH sensitivities of two samples, one with an oxide thickness t_{tox} of 60 nm and the other with 40 nm.

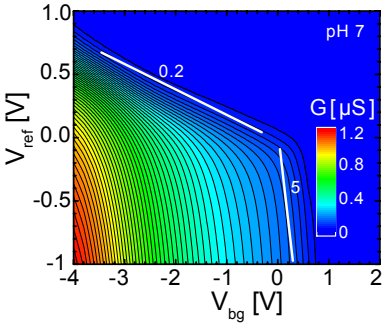

Figure A.2: Two-dimensional conductance (G) map for a fixed pH value of 7. G is displayed together with contour lines as a function of the back-gate voltage V_{bg} and the liquid potential V_{ref}. The layer thicknesses for this device are from top to bottom $t_{Al2O3} \sim 24$, $t_{tox} \sim 40$, $t \sim 80$ and $t_{box} = 150$ nm for the Al_2O_3, top-oxide, nanowire and buried oxide layers, respectively. The white lines indicate the slope at the respective contour lines. They correspond to two different ratios of the coupling capacitance between the back- and liquid-gate.

The full 2d conductance plot of the second sample is shown in Fig. A.2. This device provided a pH-induced shift in the gate threshold of 220 mV/pH when measured as a function of back-gate voltage V_{bg} at a constant liquid potential of $V_{ref} = 0.5$ V. This graph is similar to the one in Fig. 3.3. The numbers next to the white lines correspond to the slope of lines of equal conductance, which is determined by the capacitance ratio between the back-gate and the liquid gate. The sensitivity value of 220 mV/pH was measured for a capacitance ratio of 0.2, which when multiplied corresponds to 44 mV/pH relative to the liquid potential.

A.3 pH sensitivity in the inversion regime

In this thesis we focused on the accumulation regime of our fabricated ambipolar nanowire FETs. To round out the capabilities of our sensor, we show in Fig. A.3a the 2d conductance map in the inversion regime at pH=5. The visible kink can be explained with the same reasoning used in chapter 3. The white lines correspond to the capacitance ratio between the back-gate and the liquid gate.

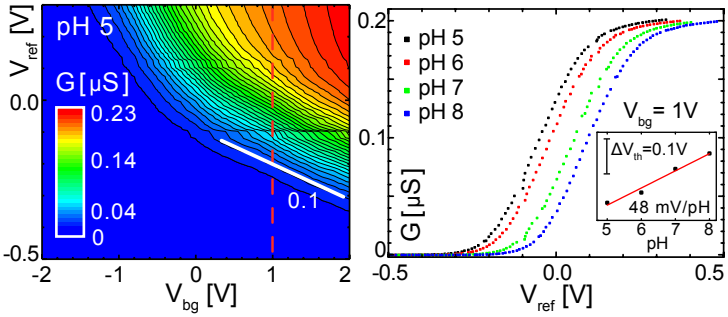

Figure A.3: **(a)** Two-dimensional conductance (G) map in the inversion regime for a fixed pH value of 5. G is displayed together with contour lines as a function of the back-gate voltage V_{bg} and the liquid potential V_{ref}. The white lines indicate the magnitude of the slope at the respective contour lines. The dashed red line highlights the parameter range that was used in the cut of (b). Nanowire FET fabricated from a different SOI wafer (BOX layer thickness: $t_{BOX} = 350\,nm$, device layer thickness: $t_{NW} = 60\,nm$, TOX layer thickness: $t_{TOX} \sim 20\,nm$, ALD layer thickness: $t_{ALD} \sim 12\,nm$, doping level: boron doping density $\sim 10^{16}\,\mathrm{cm}^{-3}$). **(b)** Effect of pH change on the transfer characteristics measured as a function of V_{ref} and V_{bg}. For increasing pH values the conductance curves shift to more positive gate values. Inset: Extracted pH sensitivity of $\sim$48 mV/pH.

Fig. A.3b shows a cut through the recorded 2d-G-maps in the inversion regime (dashed red line, Fig. A.3a) for a constant back-gate voltage V_{bg} of 1 V. We observe a clear shift to the right. For increasing pH values the surface potential becomes more negative, thus shifting the transfer characteristic to more positive gate values (decrease in conductance). The inset of Fig. A.3b shows the extracted threshold voltage shifts ΔV_{th} with the pH sensitivity of $\sim$48 mV/pH.

A.4 Additional passivation scheme

In chapter 3 we discussed the passivation scheme with silanes. For binding and unbinding experiments in liquid environments, the liquid potential has to be monitored. Hence integrated electrodes on portable sensing platforms are crucial elements. Solid-state reference electrodes would be of great promise in the use of such intergrateable electrodes. Recently we gained data from a methoxy-(dimethyl)-octadecyl-silane passivation. This silane has only one leg as linker (inset Fig. A.4a). It will not tend to polymerize. The long carbon chain brush should in addition prevent diffusion of protons to the surface.

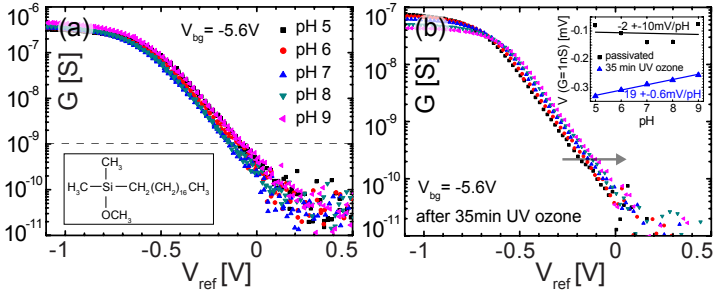

Figure A.4: Methoxy-(dimethyl)-octadecyl-silane passivation on a nanowire FET (pixel structure). **(a)** Effect of pH change on the transfer characteristics of a passivated nanowire FET measured as a function of V_{ref} and V_{bg}. No pH induced shift is visible. The inset shows the used silane (methoxy-(dimethyl)-octadecyl-silane). The dashed line highlights the conductance range that were chosen for extraction of the voltage shift. **(b)** Effect of pH change after UV ozone treatment (35 min). For increasing pH values the conductance curves shift to more positive gate values. Inset: Extracted pH sensitivities for the passivated nanowire FET ∼2 mV/pH and after UV ozone treatment ∼20 mV/pH.

Fig. A.4a shows the effect of the pH change for a passivated nanowire FET (pixel structure). While increasing the pH, hardly any shift is visible. The transfer curves measured in forward and backward direction fluctuate and do not show any trend. To remove the passivation layer a 35 min UV ozone treatment was performed. Fig. A.4b displays the effect of increasing pH values after the treatment. A slight shift to the right is visible. For clearness only the forward direction is shown. To extract the sensitivities we choose a constant conductance level of 1 nS (dashed line in Fig.A.4a) and extracted the voltages for each transfer curve. The inset of Fig. A.4b shows

the extracted voltage shifts V for the passivated and UV ozone treated wire. While for the passivated nanowire we extract a sensitivity of almost zero, the UV ozone treatment yields a sensitivity increase of $\sim 20\,\mathrm{mV/pH}$.

A.5 Statistics on measured pH sensitivities

In Fig. A.5 we have compiled the sensitivities we extracted from devices from different batches, which were fabricated, characterized and measured during the last three years. The minor fluctuations can be explained by small geometry changes, e.g., different ALD layer thickness, TOX layer thickness, etc. While becoming more familiar with processing nanowire FET sensors along this thesis we could increase their performance, which also can explain the slight increase of their sensitivity.

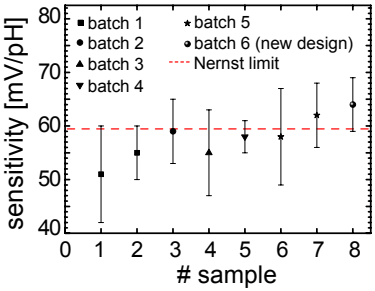

Figure A.5: Reproducibility of pH sensitivities for some devices and batches produced and measured during this thesis (batch 1 - April 2009, batch 6 - January 2011).

B
Fabrication

B.1 Electron beam versus UV lithography

Electron-beam lithography (e-beam) is a standard tool for a top-down process which allows structuring of patterns with precision and high resolution down to the few nanometer scale. These patterns are written with an electron beam into an electron-sensitive film, also known as resist, which is deposited onto the substrate. Such resists consist mostly of long chain polymers, e.g. polymethylmethacrylate (PMMA). The e-beam lithography process breaks these chains by bombarding them with high energy electrons. The shorter chains can be more easily dissolved by a developer, leaving the e-beam exposed areas uncovered by the resist. This tool has its advantages for designing a few and small structures which can be written very localized into the resist. For large scale production with many devices and big patterns it is a time consuming and a very slow technique. Each structure needs to be aligned according to the position on the substrate. For large scale lithography a similar technique can be adapted, namely the ultra-violet (UV) lithography. It uses the same principle. Instead of an e-beam sensitive resist, a 'photo'-resist is used which is sensitive to light down to the deep UV range (wavelengths below 380 nm). To transfer a pattern into the resist a photo mask is brought into contact with the photo resist. Such masks consist of a glass plate with the desired metallized pattern on it. After being exposed to a pattern of intense UV light the resist can be dissolved in a

developer. In general one talks about a positive photo resist process, if the exposed pattern remains after developing. If the unexposed patterns, which were covered by the mask remain after the developing process, on talks about a negative photo resist process. In contrast to the e-beam lithography, UV lithography has its limitation in the resolution. Structures with dimensions below one micron can only be achieved with special machines and methods, as it is used at the Intel company for their newest 45 nm and 32 nm transistor-chips [100, 101]

B.1.1 Silicon on insulator – SOI – wafers

A SOI wafer consist of three layers. The top layer is named device layer. The sandwiched middle layer consists of silicon dioxide. It is known as buried oxide (BOX) layer and its thickness can vary between a few 100 nanometer up to thicknesses in the micrometer range. This BOX layer is formed either via a SIMOX - **S**eparation by **Im**plantation of **Ox**ygen - method or by a wafer bonding method whereas the insulating layer is formed by directly bonding the oxidized silicon with a second substrate. This layer serves as insulator between the device and the lowermost layer. The bottom layer is known as substrate or handle wafer.

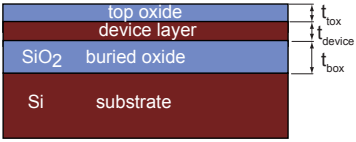

Figure B.1: SOI wafer with thermally grown top oxide. In general a SOI wafer consists of three layers, the lowermost substrate layer, the sandwiched buried oxide (BOX) layer (with thickness t_{box}) and the device layer (with thickness t_{device}). For the fabrication of our nanowires we grow an additional top oxide (TOX) layer (with thickness t_{tox}).

B.1.2 Metal mask deposition

A sufficiently large piece was cut from the SOI wafer followed by a cleaning process including acetone, Isopropanol and a UV ozone treatment. According to the fabricated structure either e-beam or negative photo resist was spin-coated and baked out on the sample (Fig. B.2b). For lithography the wafer was placed afterwards either into a scanning electron microscope (SEM) or a mask aligner. The desired structure was transferred to the substrate by exposure of the resist (Fig. B.2c). The long axis of the wires

were aligned along a <110> direction. For UV lithography a negative process was used. The unexposed resist (e-beam lithography) or the exposed photo resist (UV lithography) was then dissolved by a chemical developer (Fig. B.2d). The remaining structure served as mask during the deposition of chromium in the subsequent step. Chromium can easily be evaporated and removed selectively from the Si and SiO_2 layers by a simple etching step. Further it is easily visible under the SEM. The wafer surface was oriented perpendicular to the chromium source which was heated under vacuum by an electron beam. The evaporated metal deposits on the wafer and forms a homogeneous layers (Fig. B.2e). The thickness of the Chromium film was chosen to be as thin as possible to minimize the aspect ratio of the mask to the nanowires. As final step, the wafer was rinsed in acetone which dissolves the resist mask while leaving only the metal film in direct contact with the wafer substrate (Figs. B.2f and 1.7b).

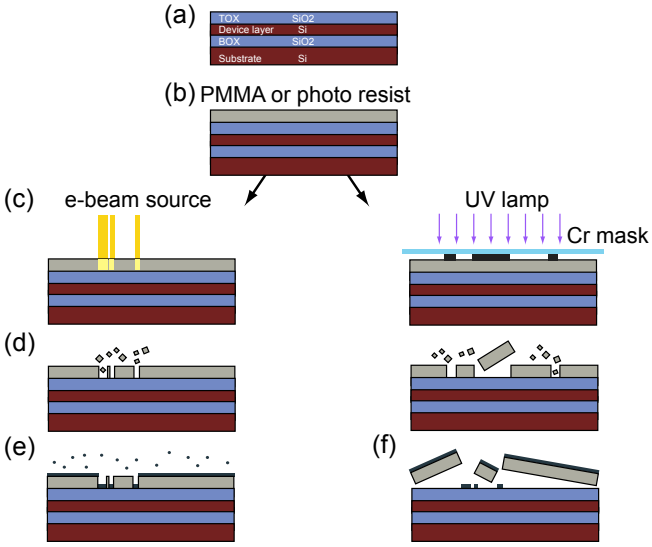

Figure B.2: Metalization process. **(a, b)** Spin coating of the SOI wafer with electron beam or photo-sensitive resist. **(c)** Patterning with e-beam or UV lithography. **(d)** Removal of the exposed (e-beam) or unexposed (negative UV lithography process) resist in a chemical developer. **(e)** Metal deposition by evaporation. **(f)** Removal of the resist mask. A structured metal film is left on the wafer's surface.

B.1.3 Etching

To transfer the chromium pattern into the TOX and the device layer, a series of dry and wet etching steps were performed to etch the alternating layers down to the BOX layer. As the first step, the wafer was placed into a plasma etcher. An initial oxygen plasma removed any leftover from the resist on the wafer's surface. Then CHF_3 plasma was used to etch the TOX layer. Here the chromium mask acts as etching mask while protecting the silicon dioxide underneath (Fig. 1.7c). Finally a second oxygen plasma step removed deposited carbon (polymer) chains from the surface. After transferring the pattern into the TOX layer, the chromium mask was selectively removed under shaking by a solution of NaOH and $KMNO_4$ in H_20 (with ratio 2:3:12) [11]. The remaining TOX pattern was then used as an etching mask to structure the device layer (Fig. 1.7d). Tetramethylammoniumhydroxide (TMAH) was chosen to etch the silicon device layer because of its selectiveness to SiO_2 and its anisotropic characteristics [26, 102, 103]. TMAH etches the (111) planes much slower than the (100) planes. To ensure no native oxide to remain as etching barrier the sample was quick-dipped into buffered hydrofluoric acid (HF, 1:20). Then the wafer was etched in an aqueous solution of TMAH and isopropanol at 45°C while vigorously stirring. The addition of isopropanol results in smother surfaces [11]. As the wires were aligned along the <110> direction, nanowires with <111> oriented side walls are formed under an angle of 54.47° (Fig. B.3). This leads to a trapezoid like shape of the wires [11].

B.1.4 Contacts

To contact the silicon nanowires a second photo-lithographic step was performed. Rectangles of 150 x 200 μm (Fig. 1.8b), or contact patterns (Figs. 1.8b, 1.8c and 5.6a) were etched into the TOX layer. Bufferd HF was used to completely remove the SiO_2 at these areas. The photo-resist acts as an etching mask. Directly after etching, the wafer had to be transferred into the evaporator to avoid formation of new native oxide. An argon sputter gun removes any new oxide formed at the contact region. Then 100 nm of aluminum was deposited with high rate at low pressure ($< 3 \cdot 10^{-7}$ mbar) onto the device layer. After lift-off the contacts were annealed in forming gas at 450° C for 30 minutes to form ohmic contacts (Fig. 1.7e).

B.1.5 Atomic layer deposition

In order to prevent leakage currents from flowing in electrolytic environments (chapter 2) the whole wafer was covered by a high quality thin aluminum oxide layer grown by atomic-layer deposition (ALD).

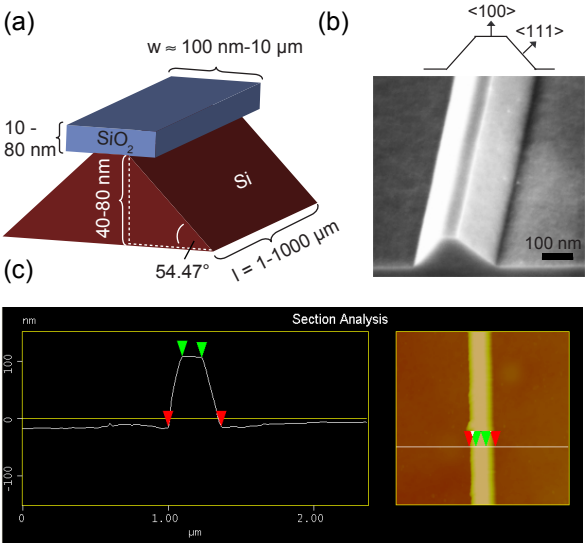

Figure B.3: **(a,b)** Geometry of a silicon nanowire. Since the nanowire patterns were aligned along the <110> direction, nanowires with <111> oriented side walls are formed. The trapezoid-shaped nanowire cross section is caused by the anisotropic etching of silicon in TMAH (SEM picture by courtesy of K. Bedner). As the silicon (111) planes are slowly etched by TMAH, nanowire side walls lie in the (111) planes, with an angle of $\sim 55^\circ$ relative to the wafer surface which are oriented into the <100> direction. The height of the wires is given by the device layer thickness. **(c)** AFM cross section and height of an e-beam written silicon nanowire. This wire was patterned by writing a 125 nm wide oblong. The final width was estimated to be $\sim$125 nm at the top (green markers) and $\sim$360 nm at the bottom (red markers) with an height of $\sim$120 nm. Picture by courtesy of B. Niesen [48].

ALD layers are conformal coatings of very high quality due to sequential layer-by-layer deposition. High quality layers can be grown at low temperatures allowing low pinhole density, uniformity over a large area and a precise thickness control [104]. For the Al_2O_3 layer water and trimethylaluminum (TMA) are used as precursors. TMA reacts through ligand exchange with the hydrogen atoms in surface OH groups; producing O-Al bonds and releasing methane. Practically all OH groups on silica and alumina react with TMA through ligand exchange, at least at temperatures between 80 and 300° C. The ALD deposition chamber was heated up and the alternating chemical reactants were introduced into the chamber as gases, supplied in

short pulses to the reactor at different times and separated by chamber evacuation. Each pulse chemically reacts with the surface thus allowing precise monolayer growth by its self-terminating reaction (Fig. B.4a-g). These steps form one cycle and can be repeated in any number. One completed cycle corresponds to a mean Al_2O_3 thickness of maximum 1.1 Å [104].

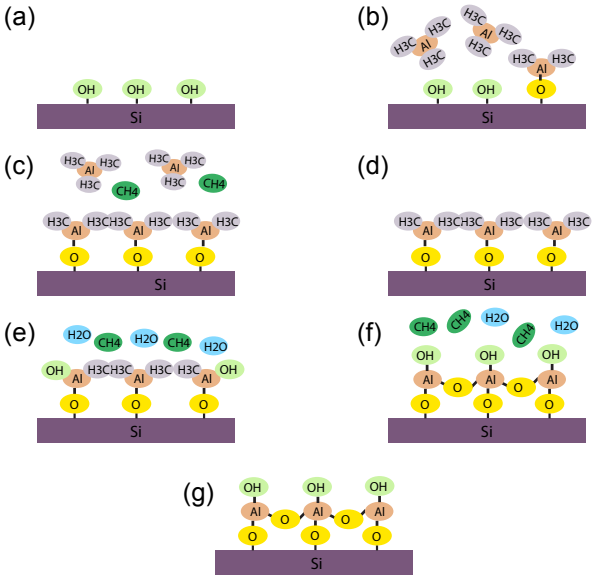

Figure B.4: Al_2O_3 deposition using ALD technique. **(a)** Silicon wafer surface with terminating OH- end-groups. **(b)** A short pulse introduces the TMA precursor into the reaction chamber. It reacts with the OH- groups producing O-Al bonds while releasing methane **(c)**. **(d)** In a next step, the unreacted TMA is pumped out. A second pulse floats the chamber with H_2O **(e)**. Water removes the CH_3 by creating Al-O-Al bridges under formation of methane **(f)** which is pumped out. **(g)** Formation of an Al_2O_3 monolayer. These steps form one cycle and can be repeated in any number.

Before placing the wafer into the ALD chamber, a short buffered HF dip was performed to remove any native oxide from the nanowire's surface. Directly afterwards, the wafer was transferred to the ALD reactor, which was subsequently heated to the required process temperature. We varied the thickness of deposited Al_2O_3 at different temperatures from 50 cycles up to 400 cycles, i.e., 5.5 nm up to 44 nm respectively (Fig. 1.7f).

B.1.6 Sealing and packaging

Once the fabrication process is finished, single devices were released from the batch for final treatments. To operate the devices in electrolyte solutions the area between the solution and the device had to be reduced to a minimum (chapter 2). Therefore a micron-sized liquid channel is defined in a resist layer (AZnlof 2070 or SU-8) by UV lithography (Fig. 1.7g). This channel runs perpendicular to the wires (Fig. 2.1). Afterwards the device was glued into a chip carrier and nanowires, on-chip electrodes as well as the back gate contacts were bonded to the pins of the carrier. Then an insulating epoxy layer (Epotek 302-3M) was deposited over the contact pads including the bonding wires to seal the whole device leaving only the liquid channel open (Figs. 1.7h and 2.1).

B.2 Optional steps

B.2.1 On-chip electrodes

On-chip electrodes allow local gating of the nanowires and could be added either as first step (before chromium evaporation) or as an follow up step after ALD. These electrodes were structured via UV lithography and aligned according to the nanowires on the wafer. After development, 5 nm titanium was evaporated as an adhesion layer followed by evaporation of 100 nm gold or platinum and the lift-off step.

B.2.2 TOX removal

During the fabrication process the TOX layer, which acted as etching mask could not be removed from the wires (Fig. B.5a). For removal an additional wet etching step in bufferd HF was performed, after patterning an etching mask via UV lithography (Fig. B.5b).

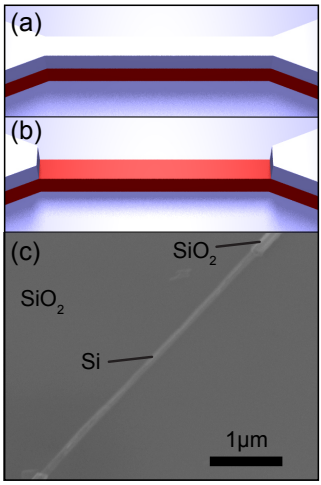

Figure B.5: Top SiO_2 removal: **(a)** Nanowire with TOX layer. **(b)** The layer can be removed after the fabrication process using a buffered HF dip. **(c)** SEM picture of a nanowire after TOX removal (revised with Photoshop).

B.3 Fabrication protocol

- **SOI wafer characteristics**

Supplier	SIMGUI Technology
Orientation	(100)
Dopant	p, Boron
Resistivity	10-20 Ωm
Device layer thickness	100 nm
BOX layer thickness	150 nm
Substrate thickness	525 μm

- **Cleaving**

Alignment	in $< 110 >$ direction
Cut	Scratch with diamond scratcher; cleave
Protection	Do not scratch TOX layer

- **Cleaning procedure**

1. Sonicate in acetone (10 min)
2. Sonicaze in 2-propanol (10 min) then dry
3. UV ozone cleaning for 10 minutes (model 42, Jelight Company)

- **UV lithography process**

1. Place wafer onto the spinner
2. Cover wafer with ma-N 415 (Micro Resist, diluted 6:1, 70% Anisol and 30% 2-methoxy-1-methylmethyl-acetat)
3. Spin to obtain 800 nm film (6000 rpm, time= 45 s, ramp= 4 s)
4. Bake out on hotplate (95°C for 90 seconds)
5. Place wafer into mask aligner (MJB-4, Suess Microtec)
6. Align chromium mask in $< 110 >$ direction of the wafer (mask obtained from Delta Mask or EPFL)
7. Expose:

Newton rings	broaden and homogeneous distributed
WEC pressure	$1.2 - 1.4$ bar
Hard contact time	6 s
Expose	10 s

8. Develop for $\sim$ 100 s in maD-323 developer

9. Evaporation of chromium in Balzers-Pfeiffer PLS 500:

Sample temperature	0°C
Base pressure	10^{-7} mbar
Rate	1-2 Å/s
Thickness	60 nm

10. Lift-off in warm acetone
11. Rinse in 2-propanol and dry

- **E-beam process**

1. Place wafer onto the spinner
2. Cover wafer with ma-N 415
3. Spin film (4000 rpm, time= 45 s, ramp= 4 s)
4. Bake out on hotplate (95°C for 90 s)
5. Place wafer into mask aligner
6. Align chromium mask in $< 110 >$ direction of the wafer
7. Expose:

WEC pressure	$1.2 - 1.4$ bar
Hard contact time	6 s
Expose	13 s

8. Develop for ~ 45 s in maD-323 developer
9. Evaporation of chromium:

Sample temperature	0°C
Base pressure	10^{-7} mbar
Rate	1-2 Å/s
Thickness	60 nm

10. Lift-off in warm acetone
11. Rinse in 2-propanol and dry
12. Place wafer onto the spinner
13. Cover wafer with PMMA (AR-P 671.09 950K from ALLRESIST, diluted)
14. Spin to obtain 350 nm film (4000 rpm, time= 40 s, ramp= 4 s)
15. Bake out in oven (180°C for 30 min)
16. Write nanowire and small contact leads with SEM (Jeol, Leo or Zeiss Supra 40)

17. Develop for 90 s in 4-methyl-2-pentanone (25 %), 2-propanol (75 %)
18. Rinse for 90 s in 2-propanol and dry
19. Evaporation of chromium:

Sample temperature	0°C
Base pressure	10^{-7} mbar
Rate	1-2 Å/s
Thickness	80 nm

20. Lift-off in warm acetone
21. Rinse in 2-propanol and dry

- **TOX layer etching**
  1. Place wafer in plasma etcher (Plasmalab^{80Plus}, Oxford)
  2. 2 min O_2 plasma (recipe for PMMA strip):

gas	O_2
flow	16
pressure 1	25 mTorr look up name
pressure 2	$5 \cdot 10^{-5}$ bar look up name
RF power	100 W

  3. 2 min 30 s CHF_3 plasma:

gas	CHF_3
flow	40
pressure 1	25 mTorr look up name
pressure 2	$5 \cdot 10^{-5}$ bar look up name
RF power	100 W

  4. 2 min O_2 plasma (recipe for PMMA strip):

gas	O_2
flow	16
pressure 1	25 mTorr look up name
pressure 2	$5 \cdot 10^{-5}$ bar look up name
RF power	100 W

- **Chromium etching**
  1. Place wafer into a beaker with etch solution (NaOH, $KMNO_4$ and deionized water, ratio 3:2:12)
  2. Shake for 10 min
  3. Place wafer in beaker with deionized water
  4. Shake for 2 min

5. Wash twice more in deionized water
6. Rinse in 2-propanol and dry

- **Native oxide etching**
  1. Dip wafer for 1 min deionized water to wet surface
  2. Dip wafer for short time ($\sim 5 - 20$ s; depends on TOX thickness) in buffered hydrofluoric acid (1:20)
  3. Wash three times in deionized water
  4. Wash in 2-propanol

- **Device layer etching**
  1. Place wafer into beaker with tetramethylammoniumhydroxide (25% in water) and 10% 2-propanol

Temperature	45°C
Stirring	Controlled vigorous stirring
Etching time	10-15 min; depends on device layer thickness

  2. Wash three times in deionized water to stop etching
  3. Wash in 2-propanol and dry

- **Contacts**
  1. Place wafer onto the spinner
  2. Cover wafer with hexamethyldisilazan (HMDS)
  3. Spin film (4000 rpm, time= 45 s, ramp= 4 s)
  4. Cover wafer with ma-N 415
  5. Spin film (4000 rpm, time= 45 s, ramp= 4 s)
  6. Bake out on hotplate (95°C for 90 seconds)
  7. Place wafer into mask aligner
  8. Align chromium mask
  9. Expose:

WEC pressure	$1.2 - 1.4$ bar
Hard contact time	6 s
Expose	13 s

  10. Develop for ~ 45 s in maD-323 developer
  11. UVO-cleaner for 5 min to remove HMDS from contact area

12. Dip wafer for short time ($\sim 30-210$ s; depends on TOX thickness) in buffered hydrofluoric acid (1:20)
13. Place wafer directly after into evaporator
14. Wait for good vacuum (base pressure $< 10^{-7}$ bar)
15. Argon sputtering:
    Program 2
    Sputtering time 30-40 s
16. Evaporation of aluminum:
    Sample temperature $-25°$C
    Base pressure $< 10^{-7}$ mbar
    Rate 5-10 Å/s
    Thickness 100-300 nm
17. Lift-off in warm Acetone
18. Rinse in 2-propanol and dry
19. Anneal in annealing oven AZ500 (MBE Komponenten GmbH):

step	temperature	time	process
1	120	60	4
2	120	600	3
3	120	600	1
4	460	35	4
5	450	600	1

- **ALD protection layer**

1. Dip wafer in buffered hydrofluoric acid (1:20) to remove native oxide (~ 10 s)
2. Wash three times in deionized water
3. Mount sample in ALD chamber (Savannah, CambridgeNanotech), pump
4. Heat up to required process temperature $T_{ALD} = 80 - 225°$C
5. Start program:

step	command	number	time
0	pulse	0	0.05
1	wait	-	12
2	pulse	$1 or 2$	0.04
3	wait	-	10
4	goto	0	$x times$

6. Wait until $T = 80°C$
7. Vent chamber, take out sample

- **Microchannel AZ2070**
  1. Place wafer onto the spinner
  2. Cover wafer with AZ 826 MIF 2070 (AZ electronic materials)
  3. Spin film (4000 rpm, time= 40 s, ramp= 4 s)
  4. Bake out on hotplate (110°C for 60 seconds)
  5. Place wafer into mask aligner
  6. Align chromium mask
  7. Expose:

WEC pressure	$1.2 - 1.4$ bar
Hard contact time	5 s
Expose	5 s

  8. Postbake on hotplate (110°C for 60 seconds)
  9. Develop for ~ 30 s in AZ 826 MIF developer (DEAZ)
  10. Resist hardening:
      a) Post exposure under mask aligner for 30 s
      b) Slowly heat up to 190°C for 10 min
      c) Slowly cool down to room temperatur $\sim$2 h

- **Microchannel SU-8**
  1. Place wafer onto the spinner
  2. Cover wafer with SU-8 2002 (Microchem Copr.)
  3. Spin film 1. (500 rpm, time= 10 s, ramp= 5 s)
  4. Spin 2. (3000 rpm, time= 30 s, ramp= 9 s)
  5. Bake out on hotplate (95°C for 60 seconds)
  6. Place wafer into mask aligner
  7. Align chromium mask
  8. Expose:

WEC pressure	$1.2 - 1.4$ bar
Hard contact time	5 s
Expose	2.5 s

  9. Postbake **immediately** on hotplate (95°C for 60 seconds)

10. Develop for $\sim$ 60 s in SU-8 developer (1-methoxy-2-propyl acetate)
11. Clean and dry in 2-propanol
12. Hardbake on hotplate (200°C for 10 min)

- **Bonding**

Model	4523 AD, CMTec
$Power_1$	1.44
$Time_1$	4
$Force_1$	1.4
$Power_2$	1.1
$Time_2$	4.8
$Force_2$	0.7
Tail	1.1
Mode	automatic

- **Epoxy sealing**
  1. Mix epoxy EPO-TEK 302-3M (EPOTEK Technologies, mixture A:B - 1:0.45)
  2. Place mixture in vacuum chamber
  3. Outgas under vacuum for 20 min
  4. Slowly seal the sample
  5. After $\sim$2.5 h close the top of the device, leaving a small opening over the microchannel
  6. Harden epoxy for 24 h at room temperature

- **Optional steps**
  1. On-chip electrodes
     a) Place device or wafer onto the spinner
     b) Cover wafer with ma-N 415
     c) Spin film (4000 rpm, time= 45 s, ramp= 4 s)
     d) Bake out on hotplate (95°C for 90 seconds)
     e) Place wafer into mask aligner
     f) Expose:

Newton rings	broaden and homogeneous distributed
WEC pressure	$1.2 - 1.4$ bar
Hard contact time	6 s
Expose	13 s

g) Develop for $\sim 45\,\mathrm{s}$ in maD-323 developer

h) Evaporation of titanium (adhesion layer):

Sample temperature	23°C
Base pressure	$8 \cdot 10^{-7}$ mbar
Rate	1-2 Å/s
Thickness	5 nm

i) Evaporation of platinum or gold:

Sample temperature	23°C
Base pressure	$8 \cdot 10^{-7}$ mbar
Rate	1-2 Å/s
Thickness	100 nm

j) Lift-off in warm acetone

k) Rinse in 2-propanol and dry

2. Silicon nanowire TOX layer etching

a) Place device or wafer onto the spinner

b) Cover wafer with (HMDS)

c) Spin film (4000 rpm, time= 45 s, ramp= 4 s)

d) Cover wafer with ma-N 415

e) Spin film (4000 rpm, time= 45 s, ramp= 4 s)

f) Bake out on hotplate (95°C for 90 seconds)

g) Place wafer into mask aligner

h) Align chromium mask

i) Expose:

WEC pressure	$1.2 - 1.4$ bar
Hard contact time	6 s
Expose	13 s

j) Develop for $\sim 45\,\mathrm{s}$ in maD-323 developer

k) UVO-cleaner for 5 min to remove (HMDS) from opened area

l) Dip wafer for short time ($\sim 30 - 210\,\mathrm{s}$; depends on TOX thickness) in buffered hydrofluoric acid (1:20)

m) Dissolve maN-415 in Aceton

n) Rinse in 2-propanol and dry

- **PDMS stamp**
  1. Mix PDMS Sylgard 184 (Dow Corning, mixture A:B - 10:1)
  2. Place mixture in vacuum chamber
  3. Outgas under vacuum for 20 min
  4. Pour mixture into mould
  5. Bake out in oven (60°C for $3 - 4$ hours)

- **Controlled oxidation**
  1. Heat oven to 100°C
  2. Dip sample in buffered hydrofluoric acid (1:20) to remove native oxide (~ 10 s)
  3. Wash three times in deionized water
  4. Place sample into oven for 10-30 min

- **Solutions**
  Titrisol, Merck
  Deionized water, Werner RO30, 18 MΩ
  DPBS, Sigma Aldrich
  Salts, Sigma-Aldrich

- **Reference electrode**
  REF200, Radiometer analytical

C Theory

In this chapter we will give a deeper insight into the theory of a field-effect transistor and the ion-sensitive FET. Note that parts of this chapter are adapted from standard literature, e.g. [8, 9].

C.0.1 Metal-semiconductor analysis

The metal-oxide-silicon (MOS) structure has been extensively studied in the the literature. We start our discussion looking at a geometry as sketched in Fig. C.1.

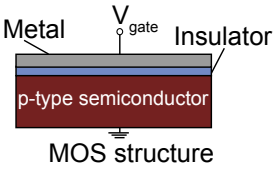

Figure C.1: Sketch of an Metal Oxide Semiconductor (MOS) structure.

The energy-band diagram of an ideal p-type MOS structure in equilibrium is shown in Fig. C.2a. For simplicity we treat the insulator as a semicon-

ductor with a very large band gap. It blocks any carrier flow between the gate metal and the semiconductor.

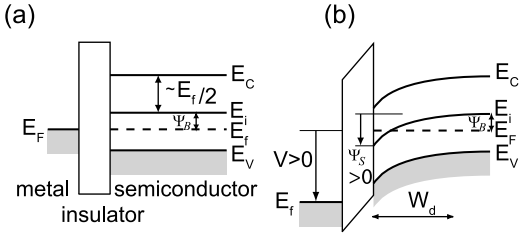

Figure C.2: Band structures of a MOS for a p-type semiconductor structure. **(a)** shows flat-band condition and **(b)** the weak inversion. Notations are given in the text. Adapted from [11].

On the left, the gate metal with its corresponding Fermi energy E_f is shown. To the right of the insulator the corresponding energy bands for the semiconductor are sketched, E_c indicates the conductance band, E_v the valence band and E_i the middle of the band gap. The potential difference between the Fermi energy of the semiconductor and the middle of the band gap is given by ψ_B. Fig. C.2a is known as the flatband diagram. Here the energy band diagram of the semiconductor is flat, hence no charge exists in the semiconductor. A finite gate voltage V_{fb} needs to be applied to obtain this case. In the ideal case V_{fb} can be written as the difference between the work function of the metal ϕ_m and the semiconductor ϕ_{Si}. However in reality trapped charges in the oxide Q_{ox} exist which contributes via the gate capacitance C_g. Hence the flatband voltage is given by

$$V_{fb} = \phi_m - \phi_{Si} - \frac{Q_{ox}}{C_g} \tag{C.1}$$

Band bending occurs only close to the surface. Deep in the bulk the bands are not influenced by the gate and ψ_b remains constant also known as the 'bulk potential'. The region where the bands are bent ('depletion layer' between surface and bulk) has a certain distribution over a 'depletion width' W_d. According to the three cases, a surface potential ψ_s with respect to the intrinsic energy level E_i of the semiconductor is built up. It is defined to be positive when the bands bend downwards.

C.0.2 Depletion width

When the surface potential is larger than zero, we have the case of depletion at the semiconductor surface (Fig. C.2b). This can be caused by an applied gate voltage. In the case of a p-type semiconductor with acceptor concentration N_a a positive gate voltage introduces positive charges to the gate which repel the positively charged holes in the semiconductor (Fig. 1.4b). A depletion region is formed where no mobile carriers remain. All the acceptors are ionized with the space charge -eN_a. The repelled charges are depleted to a depth W_d to expose sufficient negative acceptors to balance the gate charge. Hence the depletion charge can be written as $Q = -eN_aW_d$. The potential as function of distance $\psi(x)$ can be obtained by solving the Poisson equation

$$\frac{d^2\psi}{dx^2} = \frac{\rho(x)}{\epsilon_s\epsilon_0} \tag{C.2}$$

with $\rho(x)$ the total space-charge density given by the space charge eN_a, ϵ_s and ϵ_0 the permittivity of the semiconductor respectively of the vacuum. Since the potential at the interface is defined as $\psi(0)=\psi_S$ we can write the depletion width as

$$W_d = \sqrt{\frac{2\epsilon_s\epsilon_0\psi_S}{eN_a}} \tag{C.3}$$

If the depletion width becomes wide enough electrons start to appear in a very thin layer at the semiconductor surface (Fig. 1.4c) which is known as the inversion layer.

C.0.3 Debye length

The Debye length λ_D is a characteristic length for semiconductors. It gives an idea about the change of the potential according to a change in the doping profile. Lets consider the case of a voltage applied to the gate. At a certain distance - the screening distance - the Coulomb $1/r$ field is killed off exponentially and at a distance larger than λ_D there is no change in the doping profile within the semiconductor. By solving the Poisson equation (C.2) where the majority carriers taken into account we have

$$\lambda_D = \sqrt{\frac{\epsilon_s\epsilon_0 k_B T}{e\rho}}. \tag{C.4}$$

Here k_B is the Boltzmann's constant, T is the temperature, e is the unit of charge, and ρ is the relevant mobile carrier density.

C.1 MOS capacitance

When a voltage is applied to the gate of a MOS transistor a part of it will drop across the insulator V_{ox} and partially within the semiconductor Φ_s

$$V_g = V_{ox} + \Phi_s. \tag{C.5}$$

The voltage drop in the insulator is given by

$$V_{ox} = E_{ox} d = \frac{Q_s}{C_{ox}} \tag{C.6}$$

with E_{ox} being the electric field in the insulator, d the insulator thickness, Q_s the total charge per unit area in the semiconductor and C_{ox} the insulator capacitance per unit area. In the case of depletion the total capacitance C_g per unit area of the system is a series combination of the insulator capacitance and the depletion layer capacitance C_D per unit area of the of the semiconductor

$$C_g = \frac{C_{ox} C_D}{C_{ox} + C_D}. \tag{C.7}$$

The capacitance C_D depends on the applied voltage and on the frequency of charging. For the case of the depletion region this capacitance can be described as a plate capacitor with plates separated by the depletion width $C_D = \epsilon_{ox}\epsilon_0 / W_d$. In accumulation and strong inversion there is a dense layer of charge carriers close to the semiconductor-oxide interface. For this case W_d goes to zero and the total gate capacitance is dominated by the gate oxide capacitance.

C.1.1 Threshold voltage

The threshold voltage, V_{th}, of an MOS transistor is defined as the voltage which must be applied to the gate in order to form an inversion layer [8]. Starting from equation (C.5) and taking into account a nonzero flatband voltage, V_{th} can be derived [8]

$$V_{th} = V_{fb} + 2\psi_B + \frac{Q_D}{C_{ox}} \left(= V_{fb} + 2\psi_B + \frac{\sqrt{4\epsilon_s e N_a \psi_B}}{C_{ox}} \right). \tag{C.8}$$

V_{th} is beyond flat-band condition while Q_D defines the total depletion layer charge per unit area. It can be either positive or negative depending on the doping concentration N_a, the material properties and the sample specific properties.
With the derived knowledge we able know to make some assumptions about

the charge density in the inversion layer. Since it is dependent on the threshold voltage we can write the charge density per unit area in the inversion layer as:

$$Q_{inv} = C_{ox}(V_g - V_{th}) \qquad for \quad V_g > V_{th}. \tag{C.9}$$

C.2 The ISFET and the Bergveld model

For completeness we give a more detailed insight into the theory of the interaction between oxide surface of an ISFET and protons in an electrolyte. Please note that this part is slightly adapted from [6].

In case of pH, protons in the bulk solution, H_B^+, can undergo a reaction with the oxide surface. The amphoteric hydroxyl groups (-MOH) are able to donate or accept a proton. This reactions will charge the FET's surface more positively or negatively, acting as an additional gate and influencing the conducting channel beneath. The reactions can be summarized as

$$\begin{aligned} MOH &\rightleftharpoons MO^- + H_B^+ \\ MOH_2^+ &\rightleftharpoons MOH + H_B^+. \end{aligned} \tag{C.10}$$

with their associated thermodynamic equations

$$\begin{aligned} \mu_{MOH} &= \overline{\mu}_{MO^-} + \overline{\mu}_{H_B^+} \\ \overline{\mu}_{MOH_2^+} &= \mu_{MOH} + \overline{\mu}_{H_B^+}. \end{aligned} \tag{C.11}$$

Here μ and $\overline{\mu}$ represent the chemical and electrochemical potentials. $\overline{\mu}$ can be written as

$$\begin{aligned} \overline{\mu}_{H_B^+} &= \mu_{H_B^+} + e\psi_B \\ \overline{\mu}_{MOH_2^+} &= \mu_{MOH_2^+} + e\psi_S \\ \overline{\mu}_{MO^-} &= \mu_{MOH^-} - e\psi_S \end{aligned} \tag{C.12}$$

where ψ_S and ψ_B represent the electrical potentials at the oxide surface and in the bulk solution.

We can now describe the surface potential ψ_0 as

$$\psi_0 = \psi_S - \psi_B. \tag{C.13}$$

A relation between the activity of the bulk protons $a_{H_B^+}$ and the protons $a_{H_S^+}$ in the direct vicinity of the surface can be formulated using the Boltzmann equation and the surface potential to be

$$a_{H_S^+} = a_{H_B^+} e^{\frac{-e\psi_0}{k_B T}} \quad or \quad \Delta\psi_0 = 2.3\frac{k_B T}{e}(\Delta pH_S^+ - \Delta pH_B^+). \tag{C.14}$$

The dimensionless equilibrium dissociation constants are

$$\begin{aligned} K_a &= \frac{\nu_{MO^-} a_{H_S^+}}{\nu_{MOH}} \\ K_b &= \frac{\nu_{MOH} a_{H_S^+}}{\nu_{MOH_2^+}}. \end{aligned} \tag{C.15}$$

with ν_i being the density of surface states.

The surface charge density $\sigma_0 = q(\nu_{MOH_2^+} - \nu_{MO^-})$ combined with equation (C.15) and the number of sites per unit area N_S results in

$$\sigma_0 = qN_S\left(\frac{a^2_{H_S^+} - K_a K_b}{K_a K_b + K_b a^2_{H_S^+} + a^2_{H_S^+}}\right). \tag{C.16}$$

Changing now the surface pH by a small amount (∂pH_S) results in a change of the surface charge density

$$\frac{\partial\sigma_0}{\partial pH_S} = -e\beta_{int} \tag{C.17}$$

with β_{int} the intrinsic buffer capacity of the oxide surface. It is only capable to buffer small changes in the surface pH and not in the bulk pH. On the other side (and for reasons of charge neutrality) the surface charge must exist in the the electrolyte next to the surface to counter the charge which is build-up on the device surface. The charge in this double-layer,σ_{dl}, is equal to σ_0 but with opposite sign $\sigma_{dl} = -\sigma_0 = -C_{dl,i}\psi_0$. Here $C_{dl,i}$ defines the integral double-layer capacitance and can be calculated using the Gouy-Chapman-Stern model.
We define at this point the differential capacitance, which represents the ability to store charge in response to a small changes in the electrostatic potential

$$\frac{\partial\sigma_0}{\partial\psi_0} = -\frac{\partial\sigma_{dl}}{\partial\psi_0} = C_{dif}. \tag{C.18}$$

The combination of equations (C.17) and (C.18) gives the change of the surface potential due to small change of pH_S:

$$\frac{\partial\psi_0}{\partial pH_S} = \frac{\partial\psi_0}{\partial\ \sigma_0}\frac{\partial\sigma_0}{\partial pH_S} = \frac{-e\beta_{int}}{C_{dif}}. \tag{C.19}$$

As the last step we use the Nernst equation (C.14) to relate pH_S to pH_B. This yield the general equation for ISFET and its sensitivity to pH:

$$\frac{\partial\psi_0}{\partial pH_B} = -2.3\frac{k_BT}{e}\alpha \quad with \quad \alpha = \frac{1}{\frac{2.3k_BTC_{diff}}{e^2\beta_{int}} + 1} \tag{C.20}$$

A change in the bulk solution pH affects the potential at the surface which can be measured by the ISFET. α is a dimensionless sensitivity parameter varying between 0 and 1. It depends on β_{int}. For α=1, the ideal case, we will achieve the maximum sensitivity of 59.5 mv/pH at 300 K, also known as the 'Nernst limit'. We note here that β_{int} depends on the gate oxide used as interface layer.

C.3 Detailed explanation of the capacitance model

In chapter 3 we introduced a simple capacitance model to explain our results. In the following we will give a deeper insight into this model.

In equilibrium when no or only a small source-drain voltage is applied, the charge states are defined by the capacitors shown in the schematics of Fig. 3.6. For a one-dimensional system, the contact capacitance C_c should be $<< C_{NW}$ and can therefore be neglected.

Changing the charge at the surface of the nanowire by δQ_0 (Fig. C.3a), like it is be the case of altering the pH, will cause a change of the charge δQ in the nanowire itself. This charge can be influenced by V_{bg} and by V_{lg}. This scenario is sketched in Fig. C.3b for V_{bg}. The response of the charge δQ to the back-gate respectively the liquid gate can be written as

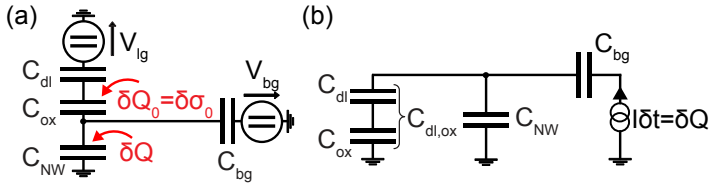

Figure C.3: **(a)** Sketch of the capacitance model where a charge δ_0 is added (or removed) to the surface of the ISFET surface causing a change of the charge δQ in the nanowire. **(b)** Influence of the back-gate on the charge δQ.

$$\begin{aligned}\frac{\delta Q}{\delta V_{bg}} &= C_{bg}\frac{C_{NW}}{C_{NW}+C_{dl,ox}+C_{bg}}\\ \frac{\delta Q}{\delta V_{lg}} &= C_{dl,ox}\frac{C_{NW}}{C_{NW}+C_{dl,ox}+C_{bg}}.\end{aligned} \tag{C.21}$$

The dependence of δQ on δQ_0 results in

$$\frac{\delta Q}{\delta Q_0} = \frac{C_{NW}C_{ox}}{C_{dl}(CNW+C_{bg}+C_{ox})+C_{ox}(C_{NW}+C_{bg})}. \tag{C.22}$$

According to the Bergveld model a change in the bulk pH will cause a change of the surface pH which, in turn, will change the surface charge density σ_0. As a result charge concentration in the conductive channel will be in- or decreased with a change of the conductance G. To correct for this effect we can back compensate with either V_{bg} or V_{lg} simultaneously to keep G constant:

$$\delta pH_S\left(\frac{\partial Q_0}{\partial pH_S}\right)\left(\frac{\partial Q}{\partial Q_0}\right)+\delta V_{gate}\left(\frac{\partial Q}{\partial V_{gate}}\right). \tag{C.23}$$

Using $\frac{\partial Q_0}{\partial pH_S} = \frac{\partial \sigma_0}{\partial pH_S} = -e\beta$, equations (C.21) and $C_S := \frac{q^2\beta}{2.3k_BT}$ the surface buffer capacity, equation (C.23) can be reshuffled to result in:

$$\delta V_{gate-change} = \delta pH_S\left(\frac{2.3k_BT}{e}\right)C_S\left(\frac{\partial Q}{\partial Q_0}\right)\left(\frac{\partial V_{gate}}{\partial Q}\right). \tag{C.24}$$

All terms in this equation are known. While the first two terms on the right side are the pH change at the surface respectively a constant value, $R = C_S(\frac{\partial Q}{\partial Q_0})(\frac{\partial V_{gate}}{\partial Q})$ is the response term of the system. With equations (C.21) and (C.22) we obtain

$$\begin{aligned} R_{lg} &= \frac{C_S}{C_{dl}} \\ R_{bg} &= \frac{C_{ox}C_{dl}}{(C_{dl}+C_{ox})C_{bg}}\left(\frac{C_S}{C_{dl}}\right) \end{aligned} \tag{C.25}$$

for the liquid-gate respectively the back-gate response. The final ratio between both gates results in

$$\frac{R_{bg}}{R_{lg}} = \frac{C_{dl,ox}}{C_{bg}} \quad or \quad R_{bg} = \frac{C_{dl,ox}}{C_{bg}} R_{lg}. \tag{C.26}$$

Publication List

Peer-reviewed papers

- *Nernst limit in dual-gated Si-nanowire FET sensors*

  O. Knopfmacher, A. Tarasov, W. Fu, M. Wipf, B. Niesen, M. Calame, and C. Schönenberger, Nano Letters **10**, 2268 (2010)

- *Signal-to-noise ratio in dual-gated silicon nanoribbon FET sensors*

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- *Dual Gated Nanowire Field Effect Transistors*

  O. Knopfmacher, D. Keller, M. Calame, and C. Schönenberger, Procedia Chemistry **1**, 678 (2009)

- *Sensitivity considerations in dual-gated Si-nanowire FET sensors*

  O. Knopfmacher, A. Tarasov, W. Fu, M. Calame, and C. Schönenberger, European Cells and Materials **20**, Suppl. 3, 140 (2010)

Poster contributions

- *Electrolyte Gated Silicon Nanowire Field Effect Transistors*
  "Frontiers in Nanoscale and Technology" in Basel, January 2008
- *Electrolyte Gated Silicon Nanowire Field Effect Transistors*
  "Nanoscience workshop" in Davos, June 2008
- *Electrolyte Gated Silicon Nanowire Field Effect Transistors*
  "NanoEurope" in St. Gallen, September 2008
- *Electrolyte Gated Silicon Nanowire Field Effect Transistors*
  "DPG Spring Meeting" in Dresden, March 2009
- *Electrolyte Gated Silicon Nanowire Field Effect Transistors*
  "Nanotechday Nordwestschweiz" in Aarau, May 2009
- *The Nernst limit in dual-gated Si-nanowire FET sensors*
  "Annual Nano-Tera Meeting" in Bern, April 2010
- *Sensitivity considerations in dual-gated Si-nanowire FET sensors*
  "3rd International NanoBio Conference" in Zurich, August 2010
- *Nernst limit and sensitivity considerations in dual-gated Si-nanowire FET sensors*
  "5th international ElecMol conference" in Grenoble, December 2010
- *Nanowire FET for versatile sensing applictions*
  "Nanotech-date Nordwestschweiz" in Baaden, March 2011

Oral presentations

- *Nanostructured Li-Ion batteries*
  seminar meeting University of Basel, February 2008
- *Nano-antennas*
  seminar meeting University of Basel, February 2009
- *Dual Gated Silicon Nanowire FETs*
  contributed talk at 23rd Eurosensors conference in Lausanne, September 2009

- *Project update NanowireSensor*
  presentation at the NanowireSensor project meeting in Bern, July 2010
- *Econophysics*
  seminar meeting University of Basel, October 2010
- *Sensing experiments with dual-gated silicon nanowire FET sensors*
  seminar talk Stanford University, February 2011
- *Sensing experiments with dual-gated silicon nanowire FET sensors*
  invited talk at the IBM T. Watson Research Center, Yorktown Heights, March 2011

Curriculum Vitæ

Oren S. Knopfmacher
Born 19^{th} of March 1983 in Rehovot, Israel

Education

- 1993 - 2002
  Lise-Meitner-Gymnasium (high school) Grenzach-Wyhlen, Germany, main topics: Mathematics and Physics

- August 2000
  Summer college at the Weizmann Institute of Science, Israel

- 2002 - 2005
  Bachelor of Science in Physics at the University of Basel

- 2005 - 2007
  Master of Science in Physics at the University of Basel
  Master thesis under the supervision of Prof. C. Schönenberger: 'Development of SOI-wafer based Nanowire Field-Effect Transistors for Sensing Applications'

- October 2007 - June 2011
  PhD in experimental Physics at the University of Basel under the supervision of Prof. C. Schönenberger: 'Sensing with Silicon Nanowire Field-Effect Transistors', (defense - 28^{th} of June 2011)

Professional positions

- 2003 - 2007
  Vice president and student council of the physics and mathematics students' representation body, University of Basel

- January 2005 - September 2007
  Novartis Pharma AG, Infrastructure for IT Projects, Basel

- October 2007 - June 2011
  Research assistant in the group of Prof. C. Schönenberger at the Physics Department of the University of Basel

Honors and awards

- April 2011
  First place at the Science Slam of the University of Basel
- June 2011
  Swiss National Science Foundation (SNSF) Fellowship

Teaching experience

- 2007 - 2009
  Tutor advanced lab for physicists
- 2009 - 2011
  Tutor physics I and physics II

For valuable lectures during my studies I am indebted to: A. Berentsen, R. Bennewitz, B. Binggeli, C. Bruder, H. Burkhart, G. Burkard, A. A'Campo-Neuen, M. Calame, T. Gyalog, S. Goedecker, H.-J. Güntherodt, M. Guggisberg, M. Grote, K. Hencken, M. Hegner, H. Hidber, H.-J. Hug, H.-C. Im Hof, B. Krusche, D. Loss, D. Masser, E. Meyer, H. Schierenbeck, C. Schönenberger, I. Sick, F.-K. Thielemann, D. Trautmann, L. Tauscher, T. Vetter, D. Zumbühl.

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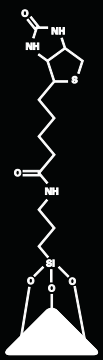

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